Analytical expression of top surface charge sensitivity in fully depleted semiconductor on insulator MOS transistor

Expression analytique de la sensibilité de la charge de surface avant pour les transistors MOS semiconducteur sur isolant complètement déplétés

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ABSTRACT. An analytical expression of free top surface charge sensitivity in FDSOI MOS structure has been established for weak inversion region and validated by TCAD numerical simulation. The influence of various FDSOI stack parameters has been analyzed. The impact of the interface trap density has been particularly emphasized, leading to a strong undesired degradation of sensitivity. This indicates that top surface passivation is a key issue for efficient charge sensing. These expressions of top surface charge sensitivity and associated threshold voltage shift should be very useful for sensor design and electrical characterization purpose.
KEYWORDS. charge sensitivity, FDSOI, threshold voltage, analytical expression.

1. Introduction

Field effect transistor (FET) based sensors are very attractive for their advantages in terms of miniaturization, integration, label-free detection and high sensitivity [BER03, STE07]. In this context, Ion Sensitive Field Effect Transistors (ISFET) have found applications as pH sensors. To improve the sensitivity of single gate ISFET, dual or double gate MOS devices with top and bottom gate electrodes have been introduced [IBA05, PAR14]. More recently, industrial grade FDSOI technology was employed to fabricate high sensitivity pH sensors, exploiting the huge front to back gate coupling in such fully depleted thin-film FET structure [MON16, RAH17]. In these FET sensors, the sensitivity is maximized when the transistor is operated in weak inversion i.e. subthreshold region, where front to back gate electrostatic coupling is not screened out by the channel formation.

Therefore, in this work, we aim at developing an analytical expression for the top surface charge sensitivity of FDSOI MOS transistors operated in weak inversion. This analytical expression could find several applications in FET sensor architecture design and electrical characterization.

2. Analytical modeling of surface charge sensitivity in FDSOI structure

In a recent paper [GHI18], we have proposed analytical expressions for the subthreshold swing in FDSOI structure. To this aim, we have considered a 1D FDSOI structure (see Fig. 1) consisting of a fully depleted silicon film of thickness t_{si} (associated capacitance C_{si}) sandwiched by a top gate oxide of equivalent thickness t_{ox2} (associated capacitance C_{ox2}) and a bottom oxide of equivalent thickness t_{ox1} (associated capacitance C_{ox1}). The bottom (resp. top) silicon channel interface features an interface trap density N_{it1} (resp. N_{it2}) with associated capacitance $C_{it1}=q.N_{it1}$ (resp. $C_{it2}=q.N_{it2}$). Gate voltage V_{g1} (resp. V_{g2}) is directly applied to the bottom gate oxide (resp. top gate oxide). For free top surface, V_{g2} is no longer applied on the top gate but is related to the top surface electric field controlled by the external charge Q_{ext} (see Eq. (1c) below). For simplicity, we assume undoped silicon film, which will have no impact on the subsequent charge sensitivity derivation.

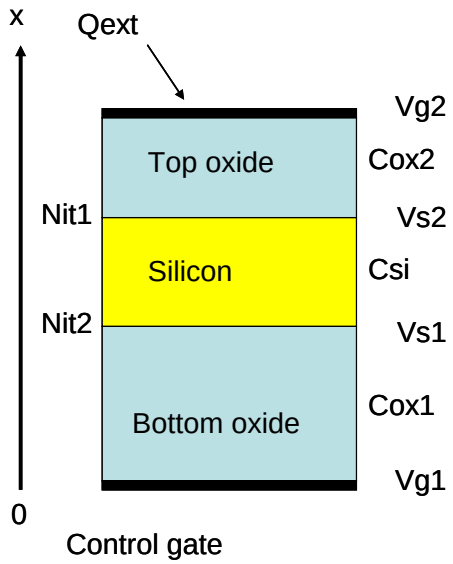

Figure 1. *Schematic of 1D FDSOI structure under consideration for analytical calculation of top surface charge sensitivity.*

Now, considering as in previous works [BAL90, WOU90, MAZ91, GHI18], that the free carrier charge in the channel can be neglected, which is of course verified in subthreshold region, and by turn, that the potential across the structure varies linearly with space, it is easy to show from Gauss's law applied at top and bottom interfaces, that the front and back surface potentials are related by:

$$V_{s1} = \frac{Q_{it1}}{C_{si} + C_{ox1}} + \frac{C_{si}}{C_{si} + C_{ox1}}.V_{s2} + \frac{C_{ox1}}{C_{si} + C_{ox1}}.V_{g1} \tag{1a}$$

$$V_{s2} = \frac{Q_{it2}}{C_{si} + C_{ox2}} + \frac{C_{si}}{C_{si} + C_{ox2}}.V_{s1} + \frac{C_{ox2}}{C_{si} + C_{ox2}}.V_{g2} \tag{1b}$$

$$V_{g2} = -\frac{Q_{ext}}{C_{ox2}} + V_{s2} \tag{1c}$$

where Q_{it1}=-q.N_{it1}.V_{s1} and Q_{it2}=-q.N_{it2}.V_{s2} are the interface trap charges, q being the absolute electron charge.

After solving the system of Eqs (1) for the unknown V_{s1} and V_{s2} one obtains:

$$V_{s1} = \frac{C_{si}.C_{ox1}.V_{g1} + C_{ox1}.C_{it2}.V_{g1} - C_{si}.Q_{ext}}{C_{si}.C_{ox1} + C_{si}.C_{it1} + C_{si}.C_{it2} + C_{ox1}.C_{it2} + C_{it1}.C_{it2}} \tag{2a}$$

$$V_{s2} = \frac{C_{si}.C_{ox1}.V_{g1} - C_{si}.Q_{ext} - C_{ox1}.Q_{ext} - C_{it1}.Q_{ext}}{C_{si}.C_{ox1} + C_{si}.C_{it1} + C_{si}.C_{it2} + C_{ox1}.C_{it2} + C_{it1}.C_{it2}}. \tag{2b}$$

Note that, in Eq. (2), we have overlooked the flat band voltage V_{fb1}. Otherwise, we should replace V_{g1} by (V_{g1}-V_{fb1}) to account for it in Eq. (2).

Following [BAL90, GHI18], the free carrier inversion charge Qi can then be obtained by integration over silicon channel as:

$$Q_i = \int_0^{tsi} q.n(x).dx = q.n_i.\frac{kT.t_{si}}{V_{s1} - V_{s2}}.\left[\exp(\frac{qV_{s1}}{kT}) - \exp(\frac{qV_{s2}}{kT})\right] \tag{3}$$

where n_i is the intrinsic carrier density.

The top surface charge sensitivity, $Sens=\delta\log(Q_i)/\delta Q_{ext}$, can be computed with no approximation using Eqs (2) and (3), providing an exact calculation for the sensitivity. But, this set of equations does not constitute a close form analytical expression for the sensitivity. Therefore, we go one step further by rewriting Eq. (3) in the form:

$$\ln(Q_i) = \ln(q.n_i.kT.t_{si}) + \frac{qV_{s1}}{kT} + \ln\left[\frac{1-\exp\left(-\frac{q\Delta V_{s12}}{kT}\right)}{\Delta V_{s12}}\right] \tag{4}$$

where $\Delta V_{s12}=V_{s1}-V_{s2}$. Moreover, noting that V_{s1} and V_{s2} are very close in weak inversion, we make a first order expansion of Eq. (4) in ΔV_{s12}, providing,

$$\ln(Q_i) \approx \ln(q.n_i.kT.t_{si}) + \frac{qV_{s1}}{kT} - \frac{q\Delta V_{s12}}{2kT} = \ln(q.n_i.kT.t_{si}) + \frac{qV_{s1}}{2kT} + \frac{qV_{s2}}{2kT}. \tag{5}$$

Then, we can evaluate the sensitivity from,

$$Sens = \frac{\delta\ln(Q_i)}{\delta Q_{ext}} = \frac{q}{2.kT}\left(\frac{\delta V_{s1}}{\delta Q_{ext}} + \frac{\delta V_{s2}}{\delta Q_{ext}}\right), \tag{6}$$

which becomes using Eq. (2),

$$Sens = \frac{q}{2.kT}\frac{2.C_{si} + C_{ox1} + C_{it1}}{C_{si}.C_{ox1} + C_{si}.C_{it1} + C_{si}.C_{it2} + C_{ox1}.C_{it2} + C_{it1}.C_{it2}}. \tag{7}$$

As will be shown below from numerical simulation, Eq. (7) does provide an improved analytical expression for the top surface charge sensitivity in bottom gate operated FDSOI structures.

Finally, it is worth evaluating the threshold voltage shift ΔV_{th} induced by the top surface external charge. To this end, we use the subthreshold swing (SW) expression found for FDSOI structure in [GHI18] and recalled in Eq. (8),

$$SW = \frac{\delta V_{g1}}{\delta\ln(Q_i)} = \frac{kT}{q}\left(1 + \frac{C_{it1}}{C_{ox1}} + \frac{(2C_{si} + C_{ox1}).C_{it2} + C_{it1}.C_{it2}}{C_{ox1}.(2C_{si} + C_{it2})}\right) \tag{8}$$

In order to derive the threshold voltage shift as $\Delta V_{th}= Sens.SW.\Delta Q_{ext}$, which leads to the expression after combining Eqs (7) and (8):

$$\Delta V_{th} = \frac{2C_{si} + C_{ox1} + C_{it1}}{C_{ox}.(2C_{si} + C_{it2})}.\Delta Q_{ext}. \tag{9}$$

In absence of interface traps i.e. $C_{it1}=C_{it2}=0$, this expression reduces to,

$$\Delta V_{th} = \frac{1}{C_{ox}}\left(1 + \frac{C_{ox}}{2C_{si}}\right).\Delta Q_{ext}. \tag{10}$$

Note that ΔV_{th} is not simply equal to $\Delta Q_{ext}/C_{ox}$ as it is often mentioned in the literature.

Moreover, looking at Eqs (7) and (10), it should be noted that the top surface charge sensitivity Sens and the associated threshold voltage shift ΔV_{th} are independent of the top oxide thickness t_{ox2}. Actually, this is due to the fact that, in the case of a free surface configuration, the top surface is field (or charge) controlled and no longer voltage controlled, fully justifying this feature.

3. Results and discussion

In order to check the validity of the new analytical expression of Eq. (7) for the sensitivity Sens, we have analyzed the influence of the FDSOI stack parameters and trap density. A nominal FDSOI structure with t_{si}=10nm, t_{ox1}=10nm and t_{ox2}=2nm was considered unless specified. The analytical results were compared to exact simulations obtained by TCAD numerical resolution of the Poisson equation under classical statistics.

3.1. *Influence of back gate oxide thickness*

Typical variations of sensitivity Sens with back gate oxide thickness t_{ox1} are illustrated in Fig. 2 as obtained from exact calculations (red solid lines) and the analytical expression of Eq. (7) for two interface trap densities with N_{it1}=N_{it2} in the case of bottom gate operated FDSOI structure (t_{si}=10nm, V_{g1}=0.01V). Note the very good agreement obtained with the analytical formula of Eq. (7), especially for large interface trap density. It is worth noting that, for zero interface trap density, the sensitivity varies linearly with t_{ox1}, whereas it saturates rapidly with t_{ox1} for large interface trap density.

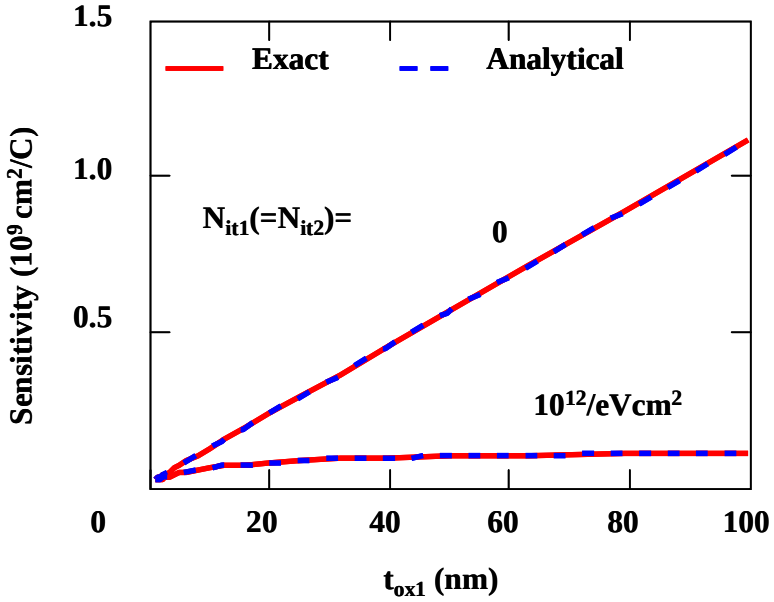

Figure 2. *Variation of sensitivity with bottom oxide thickness t_{ox1}. from exact calculations (red solid lines) and analytical expression of Eq. (7) (blue dashed lines) for two interface trap densities with N_{it1}=N_{it2} in a bottom gate operated FDSOI structure (t_{si}=10nm, t_{ox2}=2nm, V_{g1}=0.01V).*

3.2. *Influence of silicon film thickness*

Typical variations of sensitivity Sens with silicon film thickness t_{si} are given in Fig. 3 as obtained from exact calculations (red solid lines) and analytical expression of Eq. 7 (blue dashed lines) for two interface trap densities with N_{it1}=N_{it2} (t_{ox1}=10nm, t_{ox2}=2nm, V_{g1}=0.01V) in the case of bottom gate operated FDSOI structure. Note also the very good agreement achieved by the analytical equation (7), which well captures the increase of Sens with t_{si}. Similarly, the sensitivity varies almost linearly with t_{si} for zero interface trap density, whereas it tends to saturate for large interface trap density.

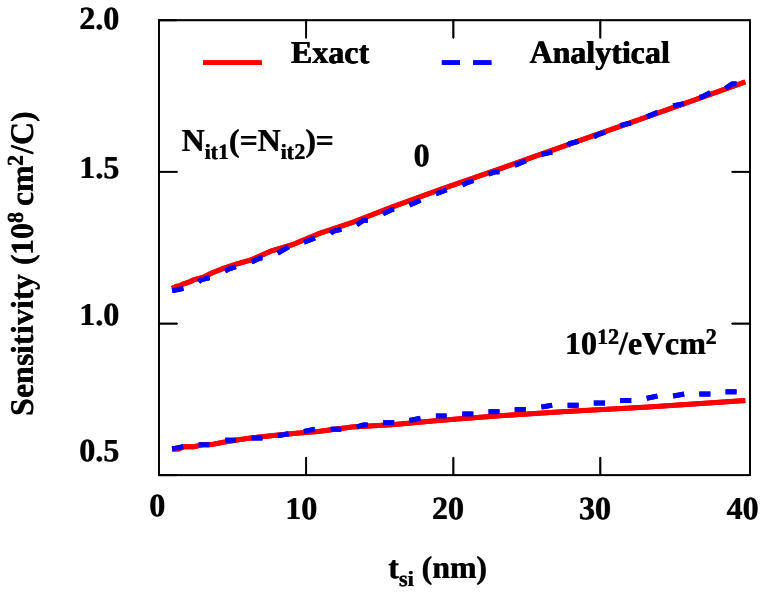

Figure 3. *Typical variations of sensitivity with silicon film thickness t_{si} from exact calculations (red solid lines) and analytical expression of Eq. (7) (blue dashed lines) for two interface trap densities with $N_{it1}=N_{it2}$ in a bottom gate operated FDSOI structure (t_{ox1}=10nm, t_{ox2}=2nm, V_{g1}=0.01V).*

3.3. *Influence of interface trap density*

Typical variations of sensitivity Sens with interface trap density ($N_{it1}=N_{it2}$) are illustrated in Fig. 4 as obtained from exact calculations (red solid lines) and the analytical expression of Eq. (7) (blue dashed lines) in the case of bottom gate operated FDSOI structure (t_{si}=10nm, t_{ox1}=10nm, t_{ox2}=2nm, V_{g1}=0.01V). Here also, one should notice the very good description of the sensitivity as a function of the interface trap density provided by Eq. (7) and its strong degradation with increasing the interface trap density.

Finally, typical variations of threshold voltage shift ΔV_{th} for $Q_{ext}=10^{11}$q/cm^2 with silicon film thickness t_{si} are illustrated in Fig. 5 as obtained from Eq. (9) for two interface trap densities $N_{it1}=N_{it2}$ in a bottom gate operated FDSOI structure (t_{ox1}=10nm, t_{ox2}=2nm). Note the noticeable reduction of the threshold voltage shift at large silicon film thickness for high trap density due to the increasing electrostatic screening of the top interface trap capacitance C_{it2} in Eq. (9).

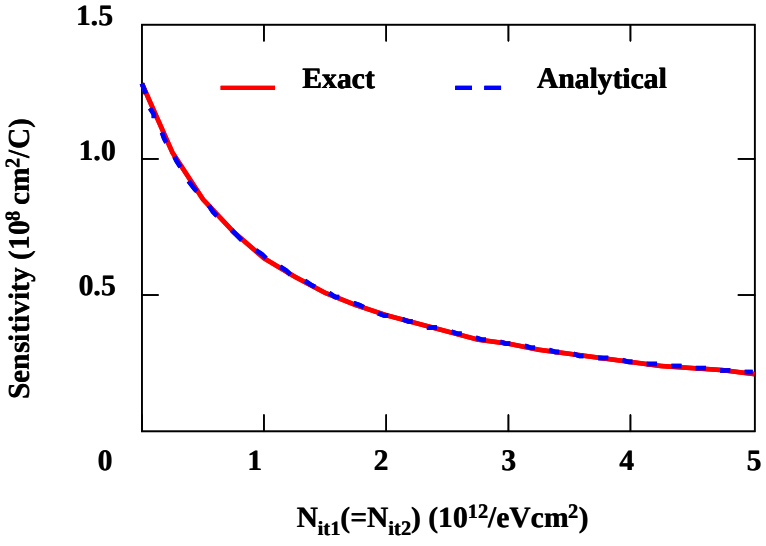

Figure 4. *Typical variation of sensitivity Sens with interface trap density ($N_{it1}=N_{it2}$) from exact calculations (red solid lines) and analytical expression of Eq. (7) (blue dashed lines) in a bottom gate operated FDSOI structure (t_{si}=10nm, t_{ox1}=10nm, t_{ox2}=2nm, V_{g1}=0.01V).*

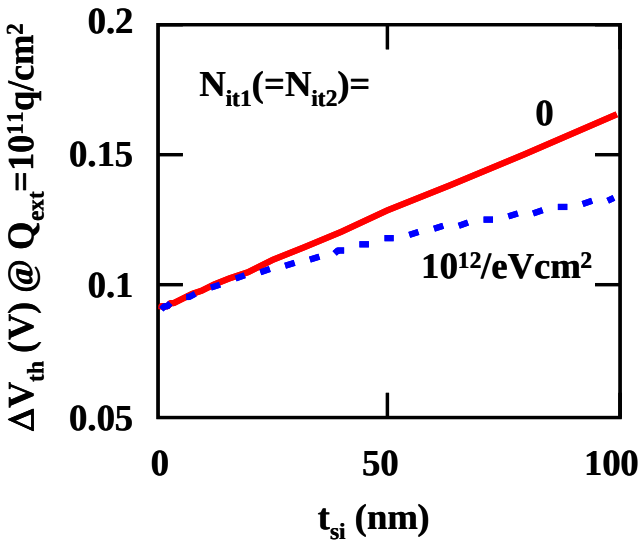

Figure 5. *Typical variations of threshold voltage shift ΔV_{th} for $Q_{ext}=10^{11}q/cm^2$ with silicon film thickness t_{si} as obtained from Eq. (9) for two interface trap densities $N_{it1}=N_{it2}$ in a bottom gate operated FDSOI structure ($t_{ox1}=10nm$, $t_{ox2}=2nm$).*

6. Conclusions

An analytical expression of the free top surface charge sensitivity in FDSOI MOS structure has been established for weak inversion region and validated by TCAD numerical simulation. The influence of various FDSOI stack parameters has been analyzed. The impact of the interface trap density has been particularly emphasized, leading to a strong undesired degradation of sensitivity. This indicates that top surface passivation is a key issue for efficient charge sensing. These expressions of top surface charge sensitivity and associated threshold voltage shift should be very useful for sensor design and electrical characterization purpose.

Acknowledgements

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