g_m/I_D based methodology for capacitive feedback LNA design

Méthodologie basée sur g_m / I_D pour la conception de LNA à retour capacitifs

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ABSTRACT. A g_m/I_D based methodology is detailed in this paper in order to help the designers to determine the optimum size of a capacitive feedback LNA by considering the design topology, the specifications to reach and the technology characteristics. Thanks to this methodology, the g_m/I_D is maximized to minimize the power consumption under design constraints which are the voltage gain, the NF and the input inductor (input Q-factor set). To illustrate this methodology, some capacitve feedback LNAs have been designed with different voltage gain requirements in 28nm FDSOI technology for 2.4GHz applications. Based on the initial parameters obtained following the different steps, three LNAs have been designed and simulated. The post-layout simulation results exhibit very good performances in terms of power consumption, linearity IIP3, bandwith BW and noise figure NF for the three given voltage gains (15dB, 18dB and 20dB). The achieved performances are quantified by high values of a well known FoM.
KEYWORDS. g_m/I_D approach, design methodology, capacitive feedback LNAs.

1. Introduction

With advanced technologies, the way of designing RF circuits is changing. In early nineties the need for low cost RF system dedicated to consumer market such as GSM pushed the RF domain in the CMOS bulk area. At this time, the f_t of the technologies was low and reaching a RF bandwidth of few gigahertzes was one of the major issues. As a result, most of RF circuits were designed in the strong inversion where the MOS transistor achieves the best f_t. As a consequence, numerous design method were developed based on Active/Triode region model valid for $V_{gs}>V_{th}$ [Vinaya 15].

However, for RF design, the paradigm is changing since advanced technologies perform very well in terms of f_t [Shameli 06]. For consumer market such as 5G and IoT, and thanks to advanced technologies, the issue is moving from the bandwidth to the power consumption since the demand is high to increase the number of services in the same mobile terminal or to provide long life communication nodes. As a consequence, the trend is to design circuit in subthreshold regions [Song 08] [Fadhuile 14]. Indeed, as presented in **Figure 1,** the efficiency of the device, which can be characterized by g_m/I_D increases as the inversion level of the channel reduces. Following this trend, several works study the optimal region of operation by considering a given function and a given technology. In [Shameli 06], a FOM based on $g_m\ f_t\ /I_D$ is introduced which allows to maximize the efficiency bandwidth product in the design of RFIC. In [Song 08], a FOM dedicated to Low Noise Amplifier (LAN) and based on g_m^2/I_D is introduced to take into consideration the NF whereas the authors in [Fadhuile 14] proposed a slightly modified FOM to add the f_t. All these approaches help the designers to choose the region of operation by considering functionalities and a technology but do not take into account the topologies and the specifications. Optimizing such FOM could lead to oversize the circuits in term of bandwidth or consumption for example.

In the nineties, g_m/I_D based methodologies have been proposed to optimize the power efficiency of several circuits such as OTA [Silveira 96]. These approaches are generally dedicated to a particular topology and allow the sizing of the transistors in all region of operation to reach given performances. To do so, the designer uses a set of equations which describe the performances of the topology and which help him determining the g_m/I_D needed to reach requirements. Then, based on abacus which gives the g_m/I_D as function of the transistor size, the topology can be sized for a given current. At this time, abacus was needed since all region models such EKV [Enz 95] or ACM [Galup 07] were not widespread. These general approaches have been used for several topologies and to optimize different performances in low frequency domain but are still quite unused in RF.

The objective of this article is to present g_m/I_D based methodologies for the design of a Capacitive Feedback LNA (CF-LNA). A method which follows the same general approach than the one presented in [Silveira 96] is given. With this method, the g_m/I_D is maximized to minimize the power consumption under design constraints which are the Gain, the NF and the input inductor which set the circuit size.

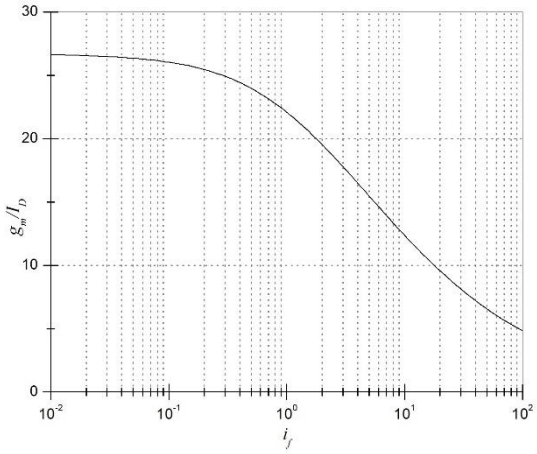


Figure 1. *g_m/I_D versus i_f in FDSOI 28nm*

2. CF-LNA Topology

The topology of the considered CF-LNA is given in **Figure 2**. The small signal gain is derived in annex and can be approximated by:

$$A_V = \frac{v_o}{v_{gs}} = -g_m R_O = -g_m \left(\frac{R_L . r_{ds}}{R_L + r_{ds}} \right) \quad [1]$$

with $R_O = r_{ds} // R_L$. A_V can be expressed in terms of the Early voltage as follow:

$$A_V = -\frac{g_m}{I_D} \left(\frac{(V_{DD} - V_{DS})(V_A + V_{DS})}{V_{DD} + V_A} \right) \quad [2]$$

A_v depends on the region of operation through the ratio g_m/I_D. For low values of V_A (i.e. $V_{DD} >> V_A$) as it is the case in advanced technologies, A_V is maximum for $V_{DSOPT} = (V_{DD} - V_A)/2$. The maximum gain A_{V_max} is then reached for:

$$r_{ds} = R_L = \frac{V_{DD} + V_A}{2 I_D} \quad [3]$$

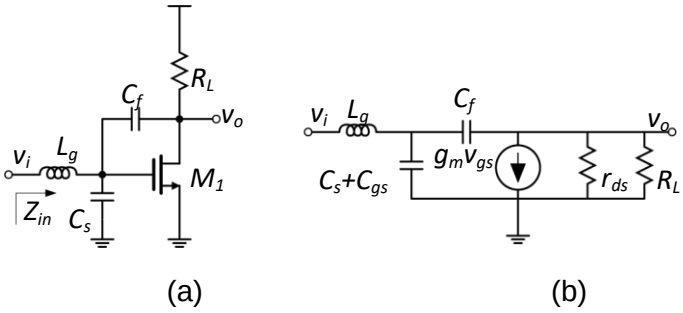
and is equal to:

$$A_{V\_max} = -\frac{g_m}{I_D} \left(\frac{V_{DD} + V_A}{4} \right) = -\frac{g_m}{I_D} . V_{EOPT} \quad [4]$$

where V_{EOPT} represent the dynamic output voltage:

$$V_{EOPT} = \left(\frac{V_{DD} + V_A}{4} \right) = R_O . I_D \qquad [5]$$

Otherwise, for non-advanced technologies, i.e. $V_{DD} << V_A$, R_L must be maximized to maximize the gain. When designing a LNA, it is first mandatory to match the input impedance to the 50 Ω antenna. As shown in annex, adding C_f feedback helps to synthesize a real part in the input impedance. An inductor is also needed to null the imaginary part and achieve the power matching. In addition, a capacitor C_s is used to add flexibility in the sizing as it will further be developed.



(a) (b)

Figure 2. *Capacitive Feedback LNA structure (a) and its small signal model (b)*

In LNA design, the NF is another requirement that must be controlled trough the design. The NF is mainly related to the g_m of the MOS as follow:

$$NF \approx 1 + \frac{\gamma}{g_m R_g} + \frac{1}{g_m^2 R_g R_O} \qquad [6]$$

We can notice that the NF depends little on the operation region since γ varies little with V_{gs}. The gain, the matching and the NF are the main requirements when designing LNA. However, other requirements can arise depending on the application like the size or the bandwidth.

3. Method for Area Reduction

The purpose of this method is to fulfill Gain and NF requirements with the smallest possible consumption while controlling the value of the L_g to limit the area of the circuit.

From [1] and [22] it is possible to express the LNA's gain as follow:

$$A_{LNA} = g_m \left(\frac{R_L . r_{ds}}{R_L + r_{ds}} \right) \sqrt{1 + Q_p^2} \qquad [7]$$

which leads to Eq. [8] of the intrinsic gain ($g_m.r_{ds}$) as a function of g_m/I_D and A_{LNA_max} obtained for V_{DSOPT}:

$$\frac{1}{g_m r_{ds}} = \frac{\sqrt{1+Q_P^2}}{A_{LNA}} - \frac{1}{g_m R_L} = \frac{\sqrt{1+Q_P^2}}{A_{LNA\_max}} - \frac{1}{2\frac{g_m}{I_D} V_{EOPT}} \qquad [8]$$

[8] is plotted for several values of gain on ***Figure 3*** for a given value of Q_p which allows the choice of L_g.

To obtain the optimal operating point, the intrinsic gain $g_m.r_{ds}$ of different transistors is plotted on the same abacus (***Figure 3***).

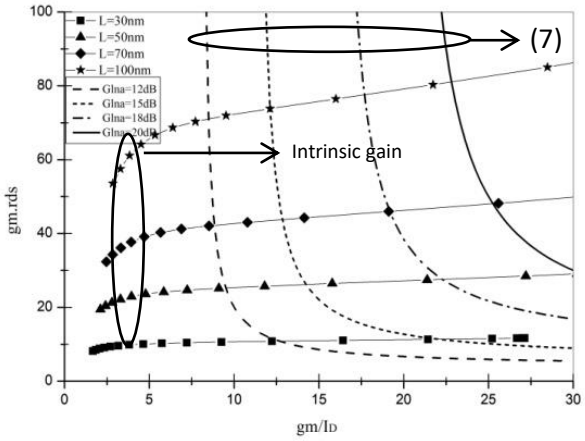


Figure 3. *$g_m.r_{ds}$ vs g_m/I_D for Q_p =1*

It is then possible to choose a value of g_m/I_D which is maximum for a required gain which finally maximizes the efficiency of the circuit.

The value of g_m is then chosen regarding the NF given by [6]. In first order approximation, NF does not depend on L neither on g_m/I_D. Then, the value of g_m/I_D, g_m and I_D are determined (for a given NF and G_V). W/L is extracted from the abacus which give $I_D/W/L(g_m/I_D)$ presented on **Figure 4** and R_O and r_{ds} are determined with [2]. As presented in equation [14] and [15], *Re(Zin)* and *Im(Zin)* only depend, at this step, on C_s and C_f which are set to have simultaneously *Re(Zin)*=50 and *Im(Zin)*=0.

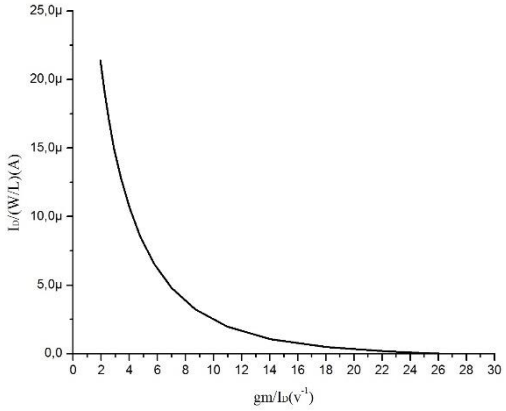


Figure 4. *$I_D/(W/L)$ vs g_m/I_D*

This method has been used to design LNAs with different voltage gain requirements in 28nm FDSOI technology for 2.4GHz applications. Results are summarized in the***Table 1***:

G_{lna} (dB)	NF (dB)	g_m (mS)	g_m/I_D (v^{-1})	L (nm)	I_D (mA)	R_0 (Ω)	W (µm)
15	<3	15	21	30	0.714	560	83
18		14	22	50	0.636	943	53
20		12	23	70	0.522	1149	54

Table 1. *LNA sizing to reach three different gain values*

In the proposed method, V_{ea} is supposed constant. However, it varies with L and g_m/I_D. To limit iteration in the method, the value of V_{ea} must be corrected as soon as the operating point is known.

4. Results

These three LNAs have been designed based on these initial parameters and considering a quality factor Q_p set to 1. Input matching is reach by adding C_f and Cs. A slight tuning has been done by simulation to refine the results. The simulation results concerning the 15dB gain LNA are shown in **Figure 5**. At 2.4GHz, the voltage gain of LNA reaches 15.7dB while NF is equal to 3dB. The IIP3 linearity is -6dBm. The LNA consumption is 760µW under 1V of power supply.

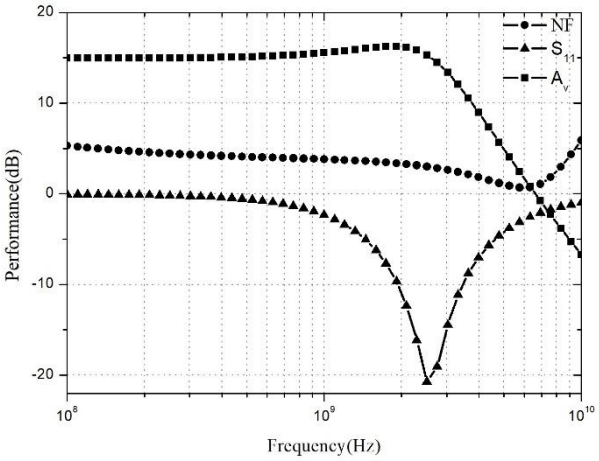


Figure 5. *Voltage gain, input matching and NF simulated results of the 15dB gain LNA*

To validate this approach, these LNAs have been designed. For measurement convenience, a matching buffer has been added at the output of the LNAs to ensure the output matching of the circuit. The silicon area occupied by this circuit (LNA + buffer) is 127µm x 170µm without pads, 400µm x 378µm with pads as illustrated in **Figure 6**.

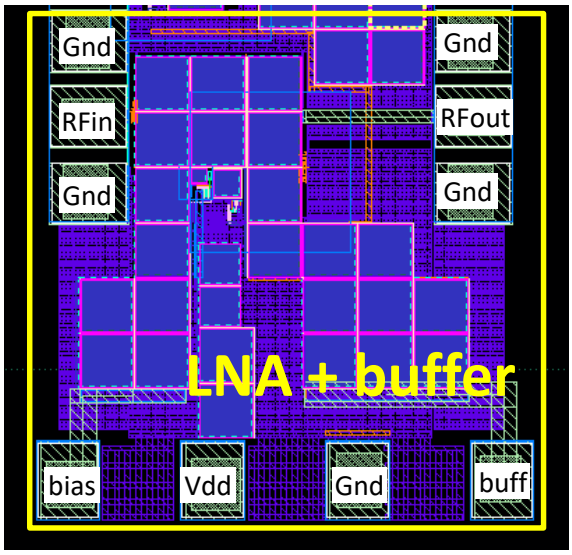


Figure 6. *Layout of the LNA with a 15dB voltage gain*

The post-layout simulation results are given in *Table 2*. Overall performances of LNAs are compared with the following FoM:

$$FoM = 20\log_{10}\left(\frac{G_{V\,av.[lin]}BW_{[GHz]}IIP3_{[mW]}}{P_{dc[mW]}\left(F_{av.[lin]}-1\right)}\right) \quad [9]$$

	Tech (nm)	Glna (dB)	NF (dB)	S11 (dB)	IIP3 (dBm)	P.Cons (mW)	BW (GHz)	VDD (V)	Lg (nH)	FOM
[Vinaya 15]	65 CMOS	8.7	3.74	-22	n/a	0.315	-	0.7	19.6+2.3+18	-
[Parvizi 15]	90 CMOS	12.6	5.5-6.5	<-10	-6~-9	7	6.9	0.5	3.1+3.1	6
[Fiorelli 14]	90 COMS	9.7	4.36	<-10	-4	0.684	0.8	1.2	0.75+11.1+10.5	8.1
[Parvizi 16]	130 CMOS	12.3	4.9-6	<-10	-11.5~-9.5	0.4	2.2	1	0	0.7
[Pan 17]	65 CMOS	21.2	2.8-4	-<-10	-7.7	2	4.3	1.2	1.5	9.25
This work	28 FDSOI (post-layout simulation)	15.7	3	-17.8	-6.75	0.76	3	1	3.8	16.7
		18.3	2.57	-20.7	-7.2	0.628	2.7			20
		19.8	2.6	-17.4	-8.5	0.55	3.4			21.68

Table 2. *Comparison performances of LNAs*

The simulated results of this capacitive feedback LNAs are compared *in Table 2* with other circuits realized and measured in the same framework. Even if this comparison is not exhaustive since only simulations are presented here, the proposed design approach seems to be attractive since the resulting FoM is very good. We especially show that gain between 15 to 20dB with NF lower than 3dB can be expected with power consumption of 0.55 to 0.76mW and with a sufficient bandwidth to address RF applications if the g_m/I_D is maximised.

5. Conclusion

Based on the g_m/I_D approach, a detailed methodology allowing the design of capacitive feedback LNAs is presented step by step. To illustrate it, some CF-LNA designs have been realized in 28nm FDSOI technology to reach a given Gv and NF at minimum power consumption for 2.4GHz applications. The post-layout simulation results show good RF performances highlighted by the FOM results. The presented methodology aims to help designers to adopt the g_m/I_D approach which is perfectly suited to determine the optimum sizes in terms of consumption for given values of specifications. Furthermore, the g_m/I_D approach appears to be well suited for advanced technologies for which the f_t is very high.

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6. Annexes

In this annex, the main equations of the CF-LNA proposed in **Figure 2** are derived. The input impedance of the structure is given by

$$Z_{IN} = L_g p + \frac{1}{C_{gs} p} // Z_M = L_g s + \frac{1}{C_{IN} p} + R_{IN} \quad [10]$$

with L_g the input inductance, C_{gs} the input parasitic capacitances of the transistor M_1, and Z_M the Miller impedance due to the capacitive feedback which can be expressed as follow if $C_f\omega << g_m$and the output capacitance C_O is much lower than C_f:

$$Z_M = \frac{1}{C_f\, p\left(1-G_v\right)} \quad [11]$$

$$A_v = \frac{v_o}{v_{gs}} = \frac{R_O\left(C_f\, p - g_m\right)}{1+R_O\left(C_f - C_O\right)p} \approx -g_m R_O \quad [12]$$

with R_O=r_{ds}//R_L . With Z_M, it is possible to express the real part and the imaginary part of Z_{in} as follow if C_L<<C_f

$$Z_M \approx \frac{1}{C_f\, p\left(1+g_m R_O\right)} + \frac{R_O}{\left(1+g_m R_O\right)} = \frac{1}{C_M\, p} + R_M \quad [13]$$

$$\Re(Z_{in}) = R_{IN} = R_M \frac{1+Q_S^2}{1+Q_P^2} \approx \frac{1+Q_S^2}{1+Q_P^2}\frac{R_O}{\left(1+g_m R_O\right)} \quad [14]$$

$$\Im m(Z_{in}) = L_g\, p + \frac{Q_p^2}{\left(C_s + C_{gs} + C_p\right)p\left(1+Q_p^2\right)} \quad [15]$$

with :

$$Q_s = \frac{1}{C_f R_O \omega_0} = \frac{1}{C_M R_M \omega_0} \quad [16]$$

$$Q_P = C_T R_P \omega_0 = \left(C_P + C_{gs} + C_s\right) R_P \omega_0 = \frac{1}{R_{IN} C_{IN} \omega_0} \quad [17]$$

$$R_P = \left(1+Q_S^2\right) R_M = \left(1+Q_P^2\right) R_{IN};\; C_P = \frac{Q_S^2}{\left(1+Q_S^2\right)} C_M \quad [18]$$

The gain of the structure depends on the small signal voltage gain A_V and the input Q-factor Q_e as follow:

$$A_{LNA} = \frac{V_o}{V_i} = A_V\sqrt{1+Q_P^2} = A_V\sqrt{1+Q_S^2}\,\frac{R_M}{R_{IN}} \quad [19]$$

where

$$Q_P = \frac{L_g \omega_0}{R_g} \quad [20]$$

The NF of a CF-LNA is given as follow for Q_e =0:

$$\begin{aligned} NF &= 1 + \frac{\gamma g_m\left(1+\left(R_g C_f \omega_0\right)^2\right)}{R_g\left(g_m{}^2 + \left(C_f\omega_0\right)^2\right)} + \frac{\left(1+\left(R_g C_f \omega_0\right)^2\right)}{R_g R_O\left(g_m{}^2 + \left(C_f\omega_0\right)^2\right)} \\ &\approx 1 + \frac{\gamma}{g_m R_g} + \frac{1}{g_m^2 R_g R_O} \end{aligned} \quad [21]$$

where R_g is the source impedance and γ is the noise excess factor which is technology dependent.

At least, the bandwidth (BW) of CF-LNA is mainly imposed by the feedback capacitor C_f in parallel with C_{gd} and the capacitors at the output node (C_O) and can be approximated as follow:

$$BW = \frac{1}{2\pi R_O\left(C_f + C_{gd} + C_O\right)} \approx \frac{1}{2\pi R_O\left(C_f + C_O\right)} \quad [22]$$

if we neglect the C_{gd}.

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