22FDX® Technologies for Ultra-Low Power IoT, RF and mmWave Applications

Technologies 22FDX® pour les Applications très basse puissance IoT, RF et Ondes Millimétriques

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ABSTRACT. In this work we revisited the 22nm FDSOI technology for lowest power IoT, RF and mmWave applications. Ultra-low leakage and power devices are described, as part of the 22FDX® portfolio. Transistors performance is presented. N-FET (p-FET) drive current of 910µA/µm (856µA/µm) at 0.8V and 100pA/µm I_{off} are reported fulfilling the requirements for ultra-low power and leakage design space. Excellent low noise is shown due to the suppressed RDF coming from the un-doped silicon channel. Superior f_T and f_{max} have been measured on CMOS and LDMOS devices. 347GHz n-FET f_T and 371GHz f_{max} were achieved on thin oxide CMOS devices. Simple PA circuit results are reported to highlight the benefit of 22FDX® technology for RF and mmWave applications. In conclusion, an outlook of the scalability as well as novel process integrations are discussed.
KEYWORDS. CMOS, FDSOI, analog, mixed-signal, RF, mmWave, ultra-low power, ultra-low leakage, RTS, LFN.

1. Introduction

Rising manufacturing costs and emerging applications require unparalleled energy efficiency and driving the need for new semiconductor device solutions [Pat 98]. An increase in the cost per die was observed with the introduction of 14/7nm FinFET technologies due to increased process complexity and mask count. Cost sensitive IoT and mobile applications drive new requirements such as increased integration, advanced power management and high RF/mmWave performance. Consequently, differentiated technologies have continually received and increased focus from the major design and foundry players [Pat 98].

The Fully Depleted Silicon-On-Insulator (FDSOI) transistor architecture has inherent electrostatic control benefits, very low mismatch capability and low parasitic capacitance, making it a powerful option to fulfil those requirements while keeping process costs and complexity low [Web 15, Maz 11]. 22FDX® technology is proven to be a versatile platform, able to co-integrate a wide spectrum of devices, addressing a variety of market segments including Mobile, IoT, analog and RF/mmWave [Car 16].

In this work we revisit the 22FDX® technology as a solid platform offer. A review of the integration process and core IoT FET performances is presented in section 2 and 3. Section 4 highlights the differentiation of the 22FDX® technology. Ultra-low leakage and power devices are discussed in section 4.1 followed by a summary of low frequency noise performance (sec. 4.2). RF and mmWave results, which are obtained on single device and circuit are discussed in sections 4.3 - 4.5. In conclusion, section 5 gives an outlook on how new integration schemes will extend the 22nm FDSOI platform technology in the future.

2. Process Integration

The 22FDX® technology leverages about 75% of the 28nm bulk technology processes enabling a high yield capability [Car 16]. Maximum die scaling is achieved compared to 28nm bulk technologies with the use of double-patterning steps in the Mid/Back-End-of-Line leading to an optimum trade-off

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between performance and costs. A high-level process flow overview is given in Figure 2.1. The main process differences are highlighted compared to the 28nm bulk technology. Four major modules have been optimized to pursue the technology scaling (highlighted boxes).

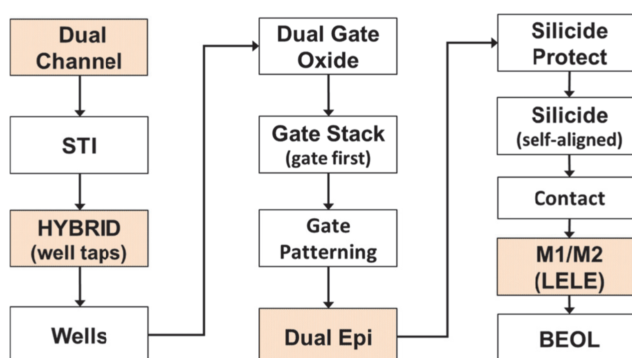

Figure 2.1. *High level 22FDX® technology process flow. Highlighted boxes indicating the major differences to 28nm bulk [Car 16]*

A Silicon-On-Insulator (SOI) substrate is employed leading to superior electrostatic control with limited short-channel effects and minimizing the device leakages [Cri 95]. Ultra-thin Si and SiGe channels are used to boost the n- and p-FET performance of the IoT devices. To enable the Back Bias (BB) capability as well as the implementation of classical passive devices a post STI hybrid etch process is performed. Furthermore, it also allows the implementation of other devices such as bipolar, HV, LDMOS or eFUSE as well as tap-cells in the bulk substrate (hybrid area) leading to maximal flexibility [Car 16]. Figure 2.2 shows the co-integration of devices on SOI next to devices located in the Hybrid area.

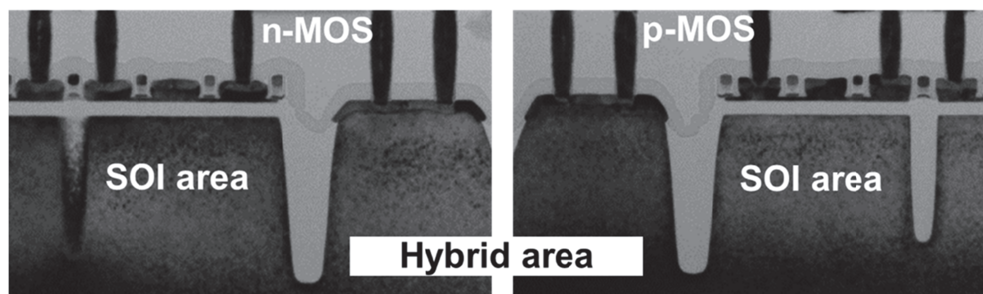

Figure 2.2. *TEM of n-MOS and p-MOS devices next to hybrid area [Car 16]*

Gate-first High-K Metal Gate (HKMG) integration ensures a maximum design and technology flexibility as well as high short channel control at 22nm gate length [Tri 16]. Low-k spacer in combination with dual in-situ doped EPI processes (Si:P and SiGe:B) allows low gate-to-drain capacitance and low access resistance to the channel [Car 16]. Technology CPP (104x) is scaled without adding extra masking steps relative to the 28nm Front-End-of-Line. Dual patterning techniques are used to scale M1/M2 pitch, leading to a logic/SRAM die scaling of 0.72x/0.83x relative to the 28 nm Poly/SiON technology node. The fully processed n-FET and p-FET IoT devices are shown in Figure 2.3.

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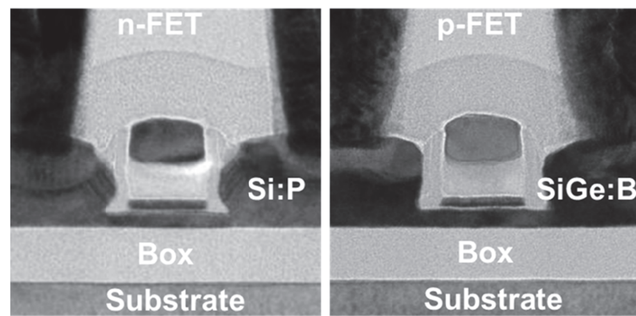

Figure 2.3. *TEM of n-FET and p-FET IoT devices of 22FDX® technology. n-FET device includes a Si channel while p-FET device features a SiGe channel [Car 16]*

3. Static Performance of IoT Devices

22FDX® technology offers the possibility to choose among a multiple threshold voltage (V_T) device suite [Car 16]. Different well configurations can be employed according to the design requirements: conventional well (RVT/HVT devices) or flip well (SLVT/LVT devices). RVT/SLVT have intrinsically un-doped conduction channel while HVT/LVT devices are lightly doped. In the so-called flip well construction n-FET devices are located on n-type back gates and p-FET devices are located on p-type back gates. Forward back biasing (FBB) can be applied to increase the device performance. In contrast, the conventional well construction enables I_{off} leakage reduction by using reverse back biasing (RBB) raising the V_T [Car 16].

Figure 3.1 shows the DC universal curve I_{DS}/I_{off} for n-FET (a) and p-FET (b) devices, respectively. Nominal transistors featuring a gate length of L = 20nm and a gate width of W = 0.17µm measured for the four different flavors. Note that p-FET devices operate always with FBB = V_D leading to a more balanced n/p ratio. Evident performance improvement is measured with FBB (2xFBB for p-FET).

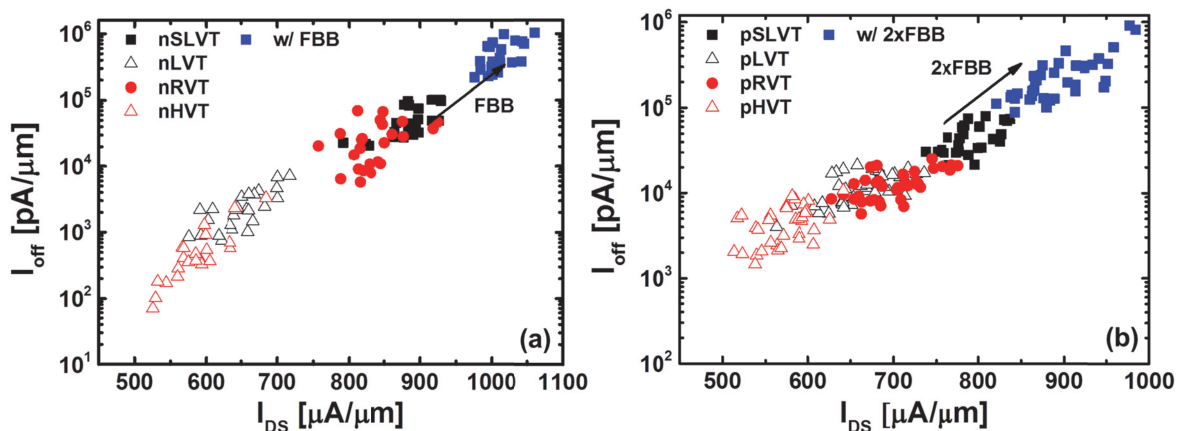

Figure 3.1. *Universal curve I_{DS}/I_{off} for n-FET (a) and p-FET (b) devices. Evident performance improvement is measured employing FBB [Car 16]*

The conduction channel in the 22nm FDSOI technology is intrinsically un-doped. The transistors are consequently immune to Random Dopant Fluctuations (RDF) effects leading to superior local mismatch [Maz 11, Tri 16]. Figure 3.2 (a) reports the Pelgrom plot for n-FET (plain symbols) and p-FET (empty symbols) devices. Excellent $A_{\Delta VT}$ slopes are measured: 1.2mV·µm for n-FET and 1.4mV·µm for p-FET, respectively [Car 16]. Standard cell-based ring oscillators have been investigated using logic test vehicles (Figure 3.2 (b)). By forward biasing the back gate FBB at V_D = 0.8V, matched ring oscillator frequency to V_D = 0.9V can be obtained. This is achieved with only a slight increase in static leakage current while dynamic leakage is reduced by 20% [Car 16]. By utilizing the inherent capability of back bias optimization in standard cells can be realized resulting in circuit level performance on a par with FinFETs.

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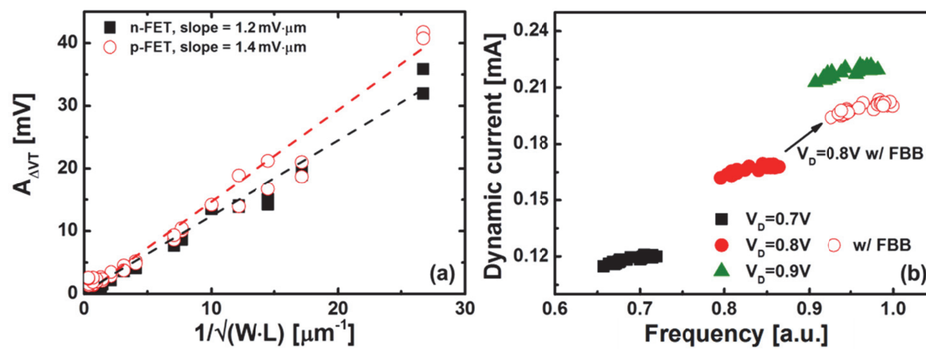

Figure 3.2. *(a) Pelgrom plot of n-FET and p-FET 22FDX® IoT devices. Excellent $A_{\Delta VT}$ slopes are reported:1.2mV·µm for n-FET and 1.4mV·µm for p-FET. (b) Dynamic current versus frequency measured on standard ring oscillator. Using FBB at V_D = 0.8V similar performance to V_D = 0.9Vare obtained [Car 16]*

4. 22FDX® Technology Portfolio: Unbeatable Differentiation

22FDX® technology offers a versatile suite of devices capable to fulfill the market requirements. A summary of the device portfolio is presented in Table 4.1 [Car 16]. To extend the technology functionality range passives devices are built in the hybrid region. It allows a higher compatibility with previous bulk technology nodes. In order to achieve superior electrostatic control with limited short-channel effect and reduced parasitic capacitances RF and mmWave transistors are built in the SOI region [Car 16]. A few examples of 22FDX® device diversification and associated performances are reported in the following sections.

Device	SOI	Hybrid	Comments
Core-FET	x		4 V_T flavors for logic and ULL
Io-FET	x		2 V_T flavors
LDMOS		x	3.3V, 5V and 6.5V
Bitcells	x		HD, HC, LV, ULV, ULL, Two-part
Resistors	x	x	Poly, diffusion, well
BJT		x	
Varactors		x	
eFUSE		x	
Diodes		x	
RF/mmWave	x		Including inductors, APMOM, etc.

Table 4.1. *22FDX® technology device suite offer. All active transistors are built on SOI whereas most of the passives are built in the Hybrid (bulk) region [Car 16]*

4.1. *Ultra-Low Leakage and Ultra Low Voltage device applications*

Power consumption is a major concern for advanced mobile applications. The 22nm FDSOI technology fulfills market requirements thanks to the possibility to co-integrate high performance IoT devices with low leakages and/or low power consumption transistors without increasing the integration complexity [Car 16]. In order to minimize the Gate Induced Drain Leakage (GIDL), the SiGe channel of p-FET devices is exchanged with a Si channel. A GIDL reduction of more than 10x can be achieved (Figure 4.1 (a)). Those devices achieve I_{off} currents < 3 pA/µm for V_{DS} = 0.8V at room temperature [Car 16]. Further I_{off} current reductions is obtained through process optimization and employing the reverse back bias RBB. Circuit functionality on logic test cells for two different libraries (8-track and 12-track heights) are demonstrated down to a minimum operating voltage of 0.38V for nominal back

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gate voltages (Figure 4.1 (b)). In both cases a V_{min} reduction (~ 150 – 300mV) is obtained compared to the 28nm reference libraries, due to the superior electrostatic properties [Car 16, Cha 18]. A further improvement is possible by utilizing the inherent technology capability of back gate biasing thus ensuring a certain gate overdrive at low V_{DD} operation due to the corresponding V_T reduction.

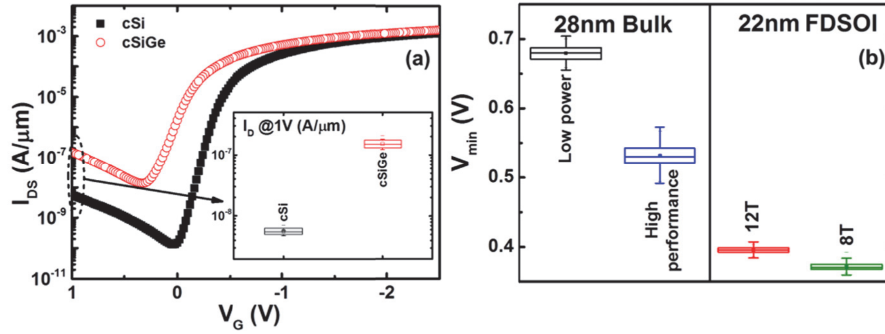

Figure 4.1. *(a) GIDL reduction by replacing SiGe channel material with Si. (b) V_{min} capability < 0.4 V is achieved in 22FDX® technology [Car 16]*

4.2. Analog & Low-Frequency Noise Performance

In state-of-the-art analog circuits area consumption and optimum performance are limited by noise [Pir 18]. Random Telegraph Noise (RTN) and Low-Frequency Noise (LFN) are the major limiting factors for circuit scalability. 22FDX® technology offers a unique possibility to modulate DC performance using back bias capability [Car 16]. The back bias is impacting the noise performance as well [Pir 18-B, The 5]. Figure 4.2 (a) shows the drain current standard deviation σI_D measured for different BB values. With negative back bias free carriers are pushed towards the top oxide interface where σI_D degrades. Using a positive BB, the carriers move towards the middle of the silicon channel leading to minimum σI_D [Pir 18, Pir 18-B]. With further back bias increase the free carriers are confined closer to the Si-BOX interface with the consequence of a σI_D degradation. Thus, optimum noise performance can be obtained employing the back bias.

Figure 4.2 (b) shows the gate bias power spectrum density (S_{Vg}) versus the measurement frequency. 22FDX® technology is benchmarked to standard 28nm bulk devices. The combination of high intrinsic gain and the use of the undoped silicon channel, which results in almost no RDF gives a strong advantage to the 22nm FDSOI technology, which over performs in LFN compared to conventional bulk devices [Pir 18]. Further S_{Vg} reduction is obtained using FBB, achieving extremely low noise levels.

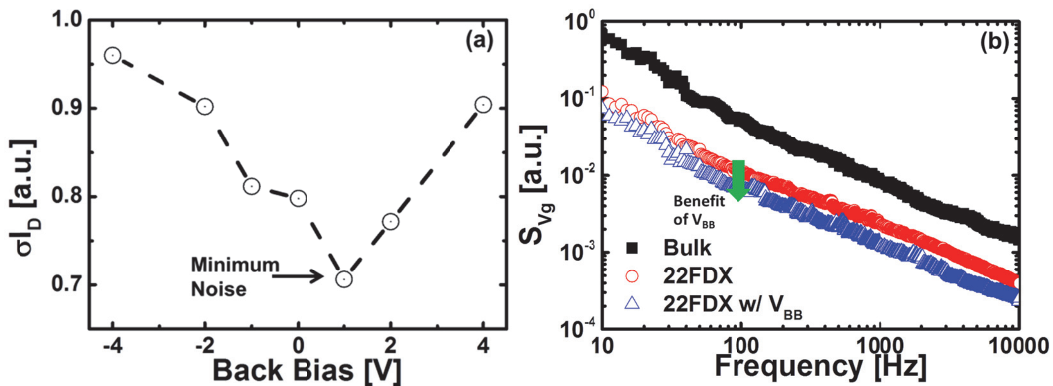

Figure 4.2. *(a) Drain current standard deviation σI_D versus back bias. Minimum noise is measured with optimized back bias. (b) Gate bias power spectrum density S_{Vg} of 22FDX® (empty symbols) and commercial bulk devices (plain symbols) versus frequency. Lower noise is measured on FDSOI devices thanks to un-doped channel and better electrostatic control [Pir 18, Pir 18-B]*

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4.3. *RF/mmWave Device Performances*

An additional advantage of the 22nm FDSOI technology compared to FinFET devices is the possibility to co-integrate high performing RF/mmWave transistors with logic devices. A superior transconductance g_m and increased self-gain g_m/g_{ds} can be obtained [Car 16, Pir 18]. Furthermore, the reduced parasitic capacitances resulting from conventional planar process technologies combined with optimized process integration for the low gate resistance leads to outstanding f_T and f_{max} performances [Ong 18].

The 22FDX® technology supports RF/mmWave FETs for both thin oxide and thick oxide device types [Ong 18]. The major figures of merit of these devices are reported in Table 4.2. The performance of the thin oxide n-FET across RF and mmWave layout is similar therefore only the standard performance is listed. Strong p-FET performance enhancement is obtained using mmWave P-cell. The peak values achieved for $f_T \cdot g_m/I_D = 2.37$ THz/V and $f_{max} \cdot g_m/I = 3.95$ THz/V are the highest ever reported [Ong 18].

	n-FET Thin Oxide (RF)	p-FET Thin Oxide (RF)	p-FET Thin Oxide (mmWave)	n-FET / p-FET Thick Oxide
f_T [GHz]	347	242	275	60 / 36
f_{max} [GHz]	371	288	299	249 / 142
f_T*g_m/I_D [THz/V]	2.37	1.7	2.05	-
f_{max}*g_m/I_D [THz/V]	3.95	3.29	3.61	-

Table 4.2. *Summary of 22FDX® RF/mmWave device performance for thin and thick gate oxide [Ong 18]*

Table 4.3 shows a benchmark of 22FDX® RF/mmWave device performance versus other commercial CMOS technologies [Ong 18]. The 22nm FDSOI technology shows an advantage over the standard bulk, FinFET or PDSOI devices. Additionally, the superior p-FET f_T and f_{max} allows a more balanced n-FET/p-FET ratio, which can lead into a symmetric design [Ong 18, Wat 17]. For the optimum circuit functionality additional elements are important. The next section shows the RF/mmWave performance of MOM capacitors and LDMOS-FETs.

	22FDX	14nm FinFET	28nm Bulk	45nm PDSOI
f_T n-FET [GHz]	347	314	310	296
f_{max} n-FET [GHz]	371	180	161	342
f_T p-FET [GHz]	242 275 (mmWave)	285	185	-
f_{max} p-FET [GHz]	288 299 (mmWave)	140	104	-

Table 4.3. *Benchmark of 22FDX® RF/mmWave performance versus available bulk/FinFET technology present in the market. 22FDX® clearly over perform the listed technologies [Ong 17]*

4.4. *MOM Capacitor and LDMOS RF Performance*

Metal-Oxide-Metal (MOM) capacitors fabricated in CMOS back-end-of-line (BEOL) interconnect layers are widely used for advanced digital, RF and mmWave applications. Figure 4.3 compares measured and simulated RF and mmWave performance of MOMs in 22FDX® technology at frequencies of 2.4, 10, 30 and 77 GHz [Shi 18]. In a specific design, there can be trade-offs between the capacitance density, Q, parasitic/shielding effect and area. Various shielding options, such as N-

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well, poly shielding and using upper 1x metal layers only can also be employed. With design optimization, a Q-factor of 80 for a 28-fF MOM capacitor at 77GHz is achieved [Shi 18].

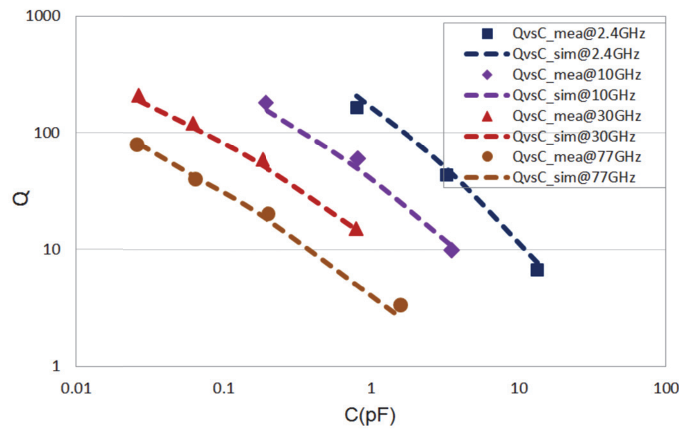

Figure 4.3. *MOM capacitor RF performance from 2.4 to 77GHz for the 22FDX® technology [Shi 18]*

Integrated circuits require devices with high breakdown voltage (B_{Vdss}) and low on-resistance ($R_{DS,on}$). Switching and RF applications require also high f_T and f_{max}. The 22FDX® technology offers a large variety of LDMOS devices [Sch 18]. The leakage of these devices is below 1 pA/µm at room temperature and the R_{DSon} is comparable with devices referenced in [Sch 18]. Additionally, the breakdown voltage has a wide margin making for a simple and easy design use. The RF performance for all devices is summarized in Table 4.4. The combination of high f_T, f_{max}, B_{Vdss}, and low $R_{DS,on}$ makes it very attractive technology for RF/mmWave and analog design. With an offering of different voltage types of the RF LDMOS circuit designers can chose an option with either higher f_T and lower $R_{DS,on}$ given by the 3.3V RF LDMOS or optimizing for higher f_{max} and operating voltages using a 5V or 6.5V RF LDMOS [Sch 18].

LDMOS	f_T [GHz]	f_{max} [GHz]	R_{DSon} [mΩ*mm²]	B_{VDss} [V]
	n-FET / p-FET	n-FET / p-FET	n-FET / p-FET	n-FET / p-FET
3.3V	55 / 24	65 /38	1.16 / 4.85	9.6 / -9.8
5.0V	42 / 21	66 / 39	1.67 / 5.98	9.7 / -9.7
6.5V	41 / 20	69 / 43	1.86 / 6.48	12.2 / -9.9

Table 4.4. *Summary of key RF and DC parameters for LDMOS devices available in 22FDX® portfolio [Sch 18]*

4.5. 22FDX®: Circuit Performance

To prove the suitability of 22FDX for mmWave applications, 28 GHz Power Amplifier (PA), switch and Low-Noise Amplifier LNA are designed and reported. The simplified circuit schematic of the 28GHz pseudo differential 2-stack PA is shown in Figure 4.4, with transformer at both the input and output for proper impedance matching. The measured performance of this PA shows a P_{1dB} of 16 dBm, a Gain of 12.7 dB and peak 41 % PAE [Che 19]. A three-stack SPST switch shows on-state insertion loss (IL) of 0.65 dB and 0.95 dB IL at 28 GHz and 40 GHz, respectively [Bal 19]. A LNA circuit was also measured, achieving a best-in-class NF = 1.46 dB with very low P_{DC} of 9.8 mW at 28 GHz [Zha 19].

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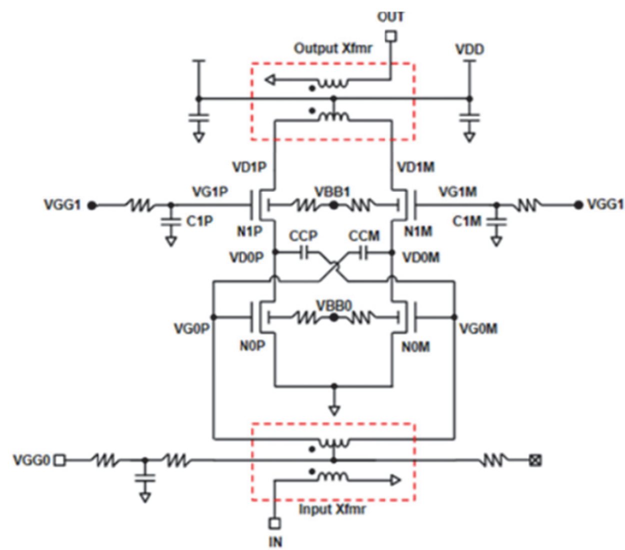

Figure 4.4. *Simplified 28GHz 5G Power Amplifier circuit schematic*

5. Scalability and Value-Added Solutions

To enrich the technology differentiation new integration elements can be employed. We report an example of optimized EPI for improved RF/mmWave performances. Employing faceted raised source/drain contacts an evident parasitic capacitance (C_{fringe}) reduction is measured without affecting the access resistance (R_{on}) (Figure 5.1 (a)). It translates directly on f_T and f_{max} boost (Figure 5.1 (b-c)) opening the way for the next steps of 22FDX® technology [Ayd 18].

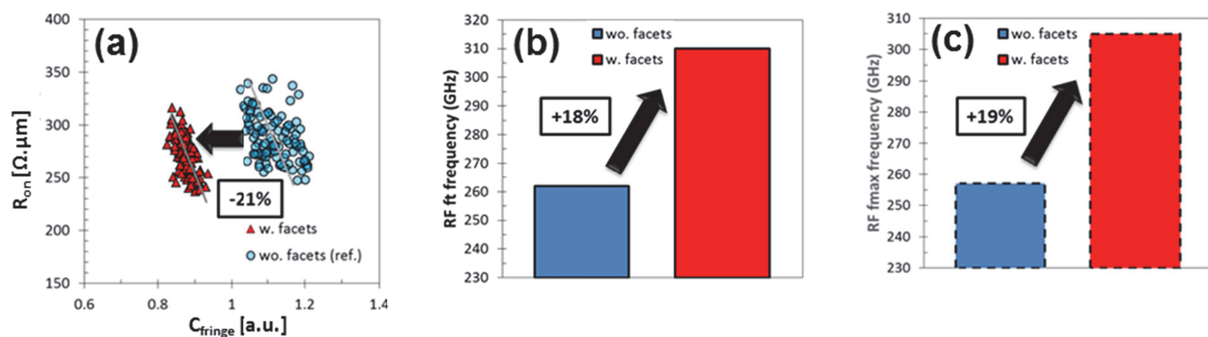

Figure 5.1. *(a) C_{fringe} reduction with the employee of faced EPI compared to standard integration scheme. The benefit directly translates on improved (b) f_T (+18%) and (c) f_{max} (+19%) [Ayd 18]*

6. Conclusions

The 22FDX® technology has been revisited with major focus on the differianting and large available portfolio. The 22nm FDSOI technology leverages out 75% of 28nm bulk process flow, leading to high yield and low costs. Optimum trade-off between performance and low-power consumption is obtained thanks to superior electrostatic control and Si channel. Intrisically un-doped channel makes also the devices immune to RDF. Thus, superior local missmatch and low-frequency noise are measured. Additionally, superior RF/mmWave results are obtained thanks to the planar construction. 347GHz (275GHz) n-FET (p-FET) f_T and 371GHz (299GHz) f_{max} were achieved on thin oxide CMOS devices. PA, LNA and switch circuit results prove the superior performance of 22FDX® technology compared to available bulk technologies.

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