Electrical characterization of advanced FDSOI CMOS devices

Caractérisation électrique des Dispositifs CMOS FDSOI avancés

G. Ghibaudo

IMEP-LAHC, Univ. Grenoble Alpes, Minatec/INPG, 3 Parvis Louis Neel, 38016 Grenoble, France, ghibaudo@minatec.inpg.fr

ABSTRACT. FDSOI technologies are very promising candidates for future CMOS circuits as they feature low variability, improved short channel effect and good transport characteristics. In this paper, we review the main electrical techniques and methodologies used to characterize the important MOS device parameters. First, the capacitance-voltage measurements are considered for the vertical stack characterization of FDSOI structures with HK/MG gate, ultra thin film channel, thin box oxide and back plane substrate. Then, the MOSFET parameter extraction methods are illustrated, as well as the transport and mobility assessment using various techniques (I-V, magneto-transport). Finally, the methodology to study the local variability of the electrical characteristics is also discussed.

KEYWORDS. FDSOI, MOSFET, parameter extraction, electrical characterization, capacitance, mobility, local variability.

1. Introduction

Fully Depleted (FD) Silicon on Insulator (SOI) technologies are interesting alternatives for future sub 28nm CMOS generations. In fact, the use of ultra thin body and buried oxide thickness (UTBB) enables better scalability, with nearly ideal subthreshold slope and low drain-induced barrier lowering (DIBL) to be achieved. Furthermore, midgap/high-k metal gate stack with low doped SOI film allows huge improvement in local variability with regard to bulk technology [FEN 07, WEB 08, SUG 08]. In this situation, precise characterization and parameter extraction methodologies are compulsory for accurate technology qualification and device modeling purpose.

For that reason, in this paper, we present the main electrical techniques and methods related to the electrical characterization of the MOSFET parameters such as vertical stack, transport parameters and local variability in advanced FDSOI CMOS devices.

2. FDSOI stack Capacitance extraction

In bulk technologies, the MOS structure is usually studied by measuring the capacitance vs gate voltage curves from depletion to accumulation region, enabling to determine the flat band voltage, the channel doping and the gate oxide thickness using the so-called Maserjian function [MAS 74, GHI 00]. This is no longer possible in FDSOI devices where full depletion takes place and where the accumulation regime cannot be generated as in bulk devices.

Though, split C-V measurements are still feasible in FDSOI MOS devices, permitting efficient parameter extraction of vertical stack parameters in FDSOI MOSFETs [BEN 13, SHI 14, NAV 15, MOH 15, MOH 18]. Especially, MOS gated diodes (see insert in Fig. 1) are also very useful devices, allowing both inversion and accumulation regimes in contrast to standard FDSOI MOS transistors [BEN 13, NAV 15].

Representative \( C_{gg}(V_g) \) characteristics obtained by split C-V measurements realized on large area (10x10\( \mu \)m\(^2\)) N and P channel of MOS gated diodes are given in Fig. 1. It should be mentioned that this FDSOI technology presents undoped 8nm Si film and 25nm BOX thicknesses. These curves have been well fitted with the capacitance model of Eq. [1],
\[ C_{gg} = \frac{bQ_iC_{ox}}{C_{ox} + bQ_i} \]  \[1\]

where \( C_{ox} \) is the front gate oxide capacitance, \( Q_i \) the inversion charge and \( b = q/(nkT) \), \( kT/q \) being the thermal voltage and \( n \) is an ideality factor. It should be noted that the validity of this capacitance model indicates that the inversion charge dependence with gate voltage follows a Lambert W function as \( Q_i(V_g) = Cox/b.LW[\exp(b.(V_g-V_t))] \), \( V_t \) being the threshold voltage [BEN 13]. The Lambert W function can be well approximated in terms of simple log and exp functions (see Eq (b) of [BEN 13]).

\[
Q_i(V_g) = \frac{Cox}{b} \ln \left( 1 + \exp\left( \frac{b(V_g-V_t)}{kT/q} \right) \right)
\]

\[2\]

\( n_i \) is the intrinsic carrier density, \( Q_{ith} = C_{ox}/(2b) \) and \( \epsilon_{si} \) the silicon permittivity. The mid position between \( V_{in} \) and \( V_{tp} \) peaks is mostly a function of the front flat band voltage \( V_{fb,f} \) and is given by [BEN 13],

\[
\frac{V_{in} + V_{tp}}{2} = V_{fb,f} + \frac{Q_d}{C_{ox1}}.
\]

\[3\]

where \( Q_d = q.N_a.t_{si} \) with \( N_a \) being the channel doping concentration and \( t_{si} \) the Si film thickness. It should be stressed that this term is negligible in low doped channels.

**Figure 1.** Experimental (symbols) and modeled (lines) \( C_{gc}(V_g) \) curves for N and P channel (MOS gated diode 10x10\( \mu \)m\(^2\), \( C_{ox} = 1.9 \mu F/cm^2 \), \( b = 25/V \)). after [BEN 13].

As shown in Fig. 2, the derivative of \( C_{gc}(V_g) \) can be employed for the determination of the threshold voltages, \( V_{in} \) and \( V_{tp} \), for N and P channels from the peak locations vs \( V_g \) (Here, \( V_{in} = 0.4V \) and \( V_{tp} = -0.7V \)). It should be noted that a very good agreement between the experimental data (symbols) and the modeling results (lines) can be obtained using Eq. [1]. Especially, the difference between \( V_{in} \) and \( V_{tp} \) is well described by the model of Eq. [2] [BEN 13],

\[
V_{in} - V_{tp} = 2\frac{kT}{q} \ln \left( \frac{Q_{ith}^2}{2q\epsilon_{si}\eta_i kT} \right) + 2\frac{Q_{ith}}{C_{ox}}
\]

where \( \eta_i \) is the intrinsic carrier density, \( Q_{ith} = C_{ox}/(2b) \) and \( \epsilon_{si} \) the silicon permittivity. The mid position between \( V_{in} \) and \( V_{tp} \) peaks is mostly a function of the front flat band voltage \( V_{fb,f} \) and is given by [BEN 13],

\[
\frac{V_{in} + V_{tp}}{2} = V_{fb,f} + \frac{Q_d}{C_{ox1}}.
\]
In scaled FDSOI technologies, the usage of ultra thin BOX down to 15-30nm permits full split C-V measurements to be realized [SHI 14]. Consequently, the gate-to-bulk capacitance $C_{gb}$ can be measured as a function of the front gate voltage as shown in Fig. 3. As it is found in bulk devices, $C_{gb}$ is also cancelling out when the channel passes into strong inversion [SHI 14]. If the silicon substrate doping concentration under the BOX is suitably large ($>10^{18}\text{cm}^{-3}$), the maximum values of $C_{gb}$ for zero back bias, $C_b$, corresponds to the series association of the gate and substrate capacitances given by $C_b=(1/C_{ox}+1/C_{si}+1/C_{box})^{-1}$. The maximum plateau value diminishes when the substrate passes into depletion with forward back biasing since the silicon substrate is here of N type. Conversely, the silicon substrate of P type would be depleted with reverse back bias. As also displayed in Fig. 3, it is also worth mentioning that the TCAD simulation of $C_{gb}$ can also be well calibrated with the experimental data.

Since the forward back biasing enables to control the space charge width in the silicon substrate or ground (back) plane (GP/BP), like in a bulk structure, it can be employed to modulate the depletion charge at the GP/BOX interface, so that the standard C-V technique for $V_{fb}$ and doping level extraction can be conducted [GHI 00]. Figure 4 shows the variation of $1/C_{gb}^2$ taken at plateau region as a function of gate voltage $V_g$. The simulation parameters used are $t_{ox}=1.4\text{nm}$, $t_{si}=7\text{nm}$, $t_{box}=30\text{nm}$, $V_{fb}=-0.27\text{V}$. After [SHI 14].
of $V_b$ when the GP is evolving from depletion to accumulation regime. In depletion regime, the slope and intercept with $1/C_{gb}^2$ ordinate enables respectively to obtain the GP doping concentration and flat band voltage $V_{fb}$ of the back gate based on Eq. [4] [SHI 14],

$$\frac{1}{C_{gb}^2} = \frac{1}{C_b^2} + \frac{2}{qN_d \varepsilon_{si}} (V_b - V_{fb,b})$$

where $N_d$ is the N-type doping concentration in the silicon substrate or GP.

![Figure 4](image1.png)

**Figure 4.** Experimental and simulated variation of $1/C_{gb}^2$ at plateau with back bias $V_b$. This plot enables extraction of the doping level of GP (BP) and $V_{fb}$ of back gate within depletion regime of GP, and $C_b$ in accumulation regime. After [SHI 14].

As can be seen from Eq. [1] and reported in Fig. 5, the variations of $Q_i/C_{gc}$ as a function of $Q_i$ well follow straight lines and by turn can be used to extract the oxide capacitance from the slope. In this case, $C_{ox}$ is extracted for two technological flavors, namely GO1 and GO2, of the gate oxide and therefore furnishes the corresponding EOT’s after correction of the dark space thickness [MOH 15].

![Figure 5](image2.png)

**Figure 5.** Experimental (symbols) and simulated (lines) variations of $Q_i/C_{gc}$ vs $Q_i$ for GO1 and GO2 gate oxide flavors. After [MOH 15].
It should also be mentioned that a better determination of the BOX thickness without any extra fitting can be conducted by directly measuring the back gate-to-channel capacitance characteristic $C_{bc}(V_b)$ as exemplified in Fig. 6 [MOH 15]. For this case, it should be emphasized that both front and back gate oxide flavors GO1 and GO2 provide in a consistent way the same maximum capacitance equal to $C_{box}$. It should also be noted that no dark space correction is necessary to obtain the buried oxide EOT since the BOX is sufficiently thick (in this case around 21nm).

![Figure 6. Experimental Cbc(Vb) characteristics variations for 2 front gate oxide flavors GO1 and GO2. After [MOH 15].](image)

It should be mentioned that a new experimental methodology based on the exploitation of the $C_{bg}(V_{gb})$ characteristics has been developed [MOH 18]. An example of such characteristics is shown in Fig. 7 and enables the whole stack equivalent thickness to be extracted as well as the flat band voltage of the well (see [MOH 18] for details). It should be noted that the $C_{gb}(V_{gb})$ of Fig. 7 has been reconstructed after several measurements of $C_{gb}(V_g)$ and $C_{gb}(V_b)$ characteristics with $V_b$ and $V_g$ as parameters, respectively. Then, the envelope of the $C_{gb}(V_{gb})$ curves is exploited to obtained the flat band voltage as on a standard C-V curve [MOH 18].

![Figure 7. Cbg versus Vgb characteristics for various Vg varying from 1V to -1.65V obtained by combining Cgb(Vg) and Cgb(Vb) characteristics. After [MOH 18].](image)

3. MOSFET parameter extraction

The precise extraction of MOSFET parameters is critical for better understanding the device operation and technology optimization, especially for ultra-scaled devices. Several methodologies have been developed for MOSFET parameter extraction but they are mostly restricted to the strong
inversion region and further consider that the inversion charge depends linearly on gate voltage overdrive [KRU 87, GHI 88, TAU 92, KAT 97, ORT 02, TAN 05, FLA 10]. Since the supply voltage $V_{dd}$ is strongly reduced with device scaling, the strong inversion approximation is becoming less and less accurate and limits the extraction to a small gate voltage range, while losing information from around threshold to sub-threshold region.

This is the reason why, new extraction procedure based on the Lambert W (LW) function, enabling the extraction of MOSFET parameters over the whole gate voltage range from 0 to $V_{dd}$, has been developed, allowing to fully take advantage of the transition from weak to strong inversion region [KAR 15]. As already mentioned in section 2, the Lambert W function is well adapted to describe the $C_{gc}(V_g)$ characteristics and, by turn, the $Q_i(V_g)$ curves as shown in Fig. 8, for n channel MOS devices from a 14nm FDSOI technology. In fact, the inversion charge is well modeled by Eq. [5] [KAR 15],

$$Q_i(V_g) = C_{ox} n \frac{kT}{q} L W \left( e^{\frac{q(V_g-V_t)}{nkT}} \right) \quad [5]$$

where $n$ is the ideality factor controlling the subthreshold slope.

![Figure 8. Experimental (solid lines) and modeled (dashed lines) $Q_i(V_g)$ characteristics of n-channel FD-SOI MOSFETs with channel width $W = 10 \mu m$ and channel length $L = 3 \mu m$. Parameters: $Cox = 2.6 \times 10^{-6} F/cm^2$, $n = 1.37$ and $V_t = 0.30 V$. After [KAR 15].](image)

In linear operation, the drain current $I_d$ of the transistor is given by:

$$I_d = \frac{W}{L} \mu_{eff} Q_i V_d \quad [6]$$

where $\mu_{eff}$ is the effective mobility and $V_d$ is the drain voltage. Moreover, using the standard degradation of the effective mobility law in strong inversion, $\mu_{eff}$ can be expressed as function of the inversion charge as:

$$\mu_{eff} = \frac{\mu_0}{1 + \theta_1 (Q_i/C_{ox}) + \theta_2 (Q_i/C_{ox})^2} \quad [7]$$

allowing the drain current to be equated to,

$$I_d = \frac{W}{L} \frac{\mu_0 Q_i V_d}{1 + \theta_1 (Q_i/C_{ox}) + \theta_2 (Q_i/C_{ox})^2} \quad [8]$$

where $\mu_0$ is the low field mobility and $\theta_1, \theta_2$ are the first and second order mobility attenuation coefficients, respectively. It should be recalled that $\theta_1=\theta_{10}+R_{sd}G_m$, with $G_m=(W/L)\cdot \mu_0 \cdot C_{ox}$ and $R_{sd}$ being the source-drain series resistance [KAR 15].

© 2018 ISTE OpenScience – Published by ISTE Ltd. London, UK – openscience.fr
As a consequence, Eqs [5] and [8] can be employed to fit the $I_d(V_g)$ characteristics over the full gate voltage range with 5 fitting parameters, namely $V_t$, $n$, $\mu_0$, $\theta_1$ and $\theta_2$ ($C_{ox}$ being extracted separately from $C_{gc}$-$V_g$ data as in section 2) using for example a Levenverg-Marquardt non-linear regression. This procedure has been used to fit $I_d(V_g)$ characteristics measured on nMOS devices from a 14 nm FDSOI technology and with varying gate lengths ($L = 18$ nm to 5 $\mu$m) as illustrated in Fig. 9. As can be seen, a very good agreement between experimental and modelled results has been achieved with a mean error of 6.5% for all gate lengths and $V_g$ values. The major MOSFET parameters, extracted using this full gate voltage range methodology, are displayed as a function of gate length in Fig. 10. For the sake of comparison, are also reported the MOSFET parameters obtained using the Y-function method, $Y(V_g)=I_d/\sqrt{g_m}$, which is limited to strong inversion region [GHI 88]. In all cases, the increase of short channel effect below $L = 30-40$ nm should be noted.

Figure 9. Experimental (solid lines) and modeled (dashed lines) $I_d(V_g)$ characteristics of n-MOS FD-SOI devices in linear (left) and logarithmic (right) scales for gate lengths $L$ ranging from 18 nm to 5 $\mu$m and gate width $W=10 \mu$m. After [KAR 15].

Figure 10. Variation of $V_t$ and $\mu_0$ (left), ideality factor $n$ (middle) and first order mobility attenuation factor $\theta_1$ (right) with gate length. Solid lines: parameters extracted from full gate voltage range methodology, dashed lines: $V_t$ and $\mu_0$ extracted using Y-function method. The ideality factor $n$ is also directly extracted from subthreshold slope (dashed line). Gate width $W=10 \mu$m. After [KAR 15].

As is usual [GHI 88], the access resistance $R_{sd}$ can be determined from the slope of the linear variation of $\theta_1$ with $G_m$ (Fig. 10). In this case, we found $R_{sd} = 840 \, \Omega \cdot \mu$m in n-MOS devices in good agreement with the values extracted from the standard Y-function method.

It should be underlined that the advantage of this full range parameter extraction methodology is that it can be employed with lower supply voltage. Indeed, it can be demonstrated that the MOSFET parameters can still be reliably determined down to $V_g$ values getting close to gate voltage where the transconductance passes through a maximum, in this case, down to 0.4-0.5 V as illustrated in Fig. 11.
As an alternative to the above-mentioned Lambert function method, a new Y-function based extraction methodology applicable from weak to strong inversion and not limited to above or near threshold region has been developed for MOSFET parameter extraction under low voltage operation [HEN 16]. However, contrary to Lambert W function, it cannot be also used as a compact model for the MOSFET. First, it has been shown that the inversion charge Qi(Vg) and the inversion capacitance Cgc(Vg) characteristics could be described analytically as a function of the Y-function from weak to strong inversion region. Thus, the drain current could be related to the Y-function as [HEN 16],

\[
\frac{Y^2}{I_d} = \frac{I_d}{g_m} = n \frac{kT}{q} \frac{Y}{\sqrt{\beta}} + \left[1 + \theta_1 \frac{Y}{\sqrt{\beta}}\right]
\]

where \(\beta = G_m V_d\) is the gain factor. Consequently, Eq. [9] indicates that the variation of \(Y^2/I_d\) \((=I_d/g_m)\) with Y should follow a parabolic behaviour with coefficients providing the three MOSFET parameters \(n, \beta\) i.e. \(\mu_0\) and \(\theta_1\). An example of such fits is illustrated in Fig. 12 as applied to a 28nm FDSOI technology [HEN 16].
Figure 12. Experimental (solid lines) and modeled (symbols) $I_d/gm(Y)$ characteristics for various gate lengths $L=28\text{nm}$ to $L=1\mu\text{m}$ ($W=1\mu\text{m}$, $Cox=1.83\times10^{-6}\text{F/cm}^2$). Gate voltage range $V_{gmax}=1\text{V}$. After [HEN 16].

All the MOSFET parameters ($\mu_0$, $\theta_1$, $n$, $V_t$), obtained using this new Y-function based method and from the standard Y-function or subthreshold slope methods with maximum gate voltage range $V_{gmax}=1\text{V}$, are shown as a function of gate length in Fig. 13. Note the consistency of the extracted parameters vs $L$ for $\mu_0$, $n$, $V_t$ and $\theta_1$. Note also that $n$ is only extracted from new Y-function method and from subthreshold slope method.

Figure 13. Variations of ideality factor $n$, $\mu_0$ and $V_t$ with gate length and $\theta_1$ with $G_m$ as obtained from new Y-function method (solid lines) and from standard Y-function or subthreshold slope methods (dashed lines) for a gate voltage range $V_{gmax}=1\text{V}$. Here, $\theta_{10}=0.3/V$ is constant with gate length.

4. Transport parameters

The carrier mobility is a key parameter determining the MOS device operation. Several techniques can be used to measure or extract the effective mobility in MOSFETs such as from $I_d(V_g)$ curves using...
e.g. Y-function [GHI 88], as in section III, by split C-V method [SOD 82, ROM 04] or from magneto-transport measurements like Hall effect [NEG 11] or magneto-resistance [MEZ 04].

The low field mobility $\mu_0$ extracted from Y-function can be investigated as a function of temperature (T) and channel length in order to identify the main scattering mechanisms in the MOS device channel. Figure 14 gives an example of $\mu_0(T)$ variations obtained in 14nm FDSOI nMOS devices [SHI 15a], illustrating the huge evolution of the scattering mechanisms with channel length. Indeed, in long channels, $\mu_0$ varies typically as $T^{-1}$, meaning that phonon scattering dominates, whereas in short channels, $\mu_0$ is lower in amplitude and nearly independent of temperature, meaning that neutral defect scattering prevails [SHI 15a].

![Figure 14](image)

Figure 14. Experimental (symbols) and modeled (lines) variation of low field mobility $\mu_0$ with temperature as obtained on nMOS devices with various gate lengths. After [SHI 15a].

In order to get a quantitative picture of the scattering behaviour with temperature, the mobility can be described by the empirical model [SHI 15a]:

$$\frac{1}{\mu_0} = \frac{1}{(300/T)\mu_{ph}} + \frac{1}{(T/300)\mu_C} + \frac{1}{\mu_{nd}}$$

which is based on Mathiessen's rule and composed with different scattering mechanisms such as phonon, Coulomb and neutral defect scattering ($\mu_{ph}$, $\mu_C$ and $\mu_{nd}$, respectively). This mobility empirical model enables a satisfactory fitting of the $\mu_0(T)$ curves (Fig. 14) and, by turn, allows to extract the variations of the different scattering mechanisms with channel length for room temperature as illustrated in Fig. 15. As can be seen from this figure, both the phonon and Coulomb mobility components are found to be independent of gate length, whereas the neutral scattering mobility $\mu_{nd}$ is clearly increasing with gate length. This behavior for $\mu_{nd}$ can be well interpreted by an exponential profile of process-induced neutral defects close to source-drain ends and featuring a critical distance of 10nm and a maximum concentration of about $8\times10^{19}\text{cm}^{-3}$ [SHI 15a]. Note also that the neutral mobility component is independent of the gate oxide thickness (GO1 and GO2), indicating that the neutral defects are located in the channel and not in the gate dielectric, emphasizing the consistency of the interpretation [SHI 15a].

The effective mobility can also be measured by the geometric magnetoresistance effect, which results from the modulation of the local carrier velocity by the Lorentz force. Therefore, after application of a high enough magnetic field B perpendicular to the gate, the channel resistance $R_{ch}$ in a large transistor ($W>5-6\times L$) is increased by the amount $\Delta R_{ch}/R_{ch}=\mu_{MR}^2 B^2$, where $\mu_{MR}$ is the so called magnetoresistance mobility. So, $\mu_{MR}$ can be measured directly without knowing the exact channel
length and is applicable below threshold [MEZ 04]. It should also be noted that $\mu_{\text{MR}}$ is not exactly equal to $\mu_{\text{eff}}$ depending on scattering mechanism and temperature [MEZ 04].

Figure 15. Variation with channel length $L_{\text{eff}}$ of the various mobility scattering components (phonons, Coulomb, neutral) for $T=300$K as obtained on nMOS devices with two gate oxide flavors. After [SHI 15a].

Figure 16 shows typical variations of the MR mobility as a function of the inversion charge density in the channel of nMOS FDSOI devices for various temperatures [CHA 06]. The mobility at low carrier density is dominated by unscreened Coulomb scattering, then passes through a maximum versus carrier density, around threshold, mainly controlled by phonon scattering, before to decrease at large inversion charge density due to surface roughness scattering [CHA 06].

Interestingly, the magnetoresistance effect can be measured not only in linear region but also as a function of drain voltage $V_d$ up to saturation region as illustrated in Fig. 17 [SHI 15b]. This means that it is possible to extract the MR mobility versus drain voltage and, by turn, to plot the variation of $\mu_{\text{MR}}$ with gate voltage for various drain voltages $V_d$ from linear to saturation region as shown in Fig. 18. It should also be noted that these MR mobility data have been very well interpreted and fitted by a semi-analytical model of drain current relying on Lambert W function. In this context, based on the gradual channel approximation, the drain current is obtained by integration along the channel of the local conductance including MR effect with an inversion charge law given by Eq. [5] and allowing to
reproduce the $\mu_{\text{MR}}$ variations with both gate and drain voltages, as shown by the dashed lines in Fig. 18 [SHI 15b].

**Figure 17.** a) Output characteristic $I_d(V_d)$ at strong inversion ($V_g = 0.9V$) for different magnetic fields $B$ from 0T to 11T at 300 K for GO1 device ($W=1\mu m$, $L=0.3\mu m$). b) Relative drain current variation ($\Delta I_d/I_d$) versus $B^2$ from linear ($V_d = 0.02V$) to saturation region ($V_d = 0.7V$). After [SHI 15b].

**Figure 18.** Experimental (symbols) and modeled (dashed lines) variation of $\mu_{\text{MR}}$ with gate voltage for various drain voltages as obtained on 14nm FDSOI nMOS devices (GO1 oxide flavor and $L=30nm$, $W=1\mu m$). After [SHI 15b].
Device variability is a serious concern for the scaling down of CMOS technologies. It is well known for many years that the threshold voltage $V_t$ and the current gain factor $\beta$ local mismatch are the main sources of local variability in MOS transistors [PEL 89, CRO 02], both impacting analog and logic circuits like SRAM cells. The introduction of undoped channel technologies such as FDSOI or FinFET has significantly lowered the $V_t$ mismatch [MAT 14, RAH 13], but it has raised new issues due to the influence of source-drain series resistance and associated variability [IOA 15, MAR 12, IOA 16].

Figure 19 shows typical set of drain current mismatch characteristics $\Delta I_d/I_d(V_g)$ obtained on nMOS paired transistors with nominal geometry from 14nm FDSOI technology. Note the huge $I_d$ mismatch below threshold (> 2-3 decades), which requires evaluating the drain current mismatch between pairs using the log difference, $\Delta I_d/I_d = \ln(I_{d1}/I_{d2})$ instead of linear difference as emphasized in [IOA 15].

The local mismatch of the associated $Y$-function, $\Delta Y/Y(V_g)$ are shown in Fig. 20. According to [IOA 15], this function allows removing the impact of $R_{sd}$ in matching analysis.

The standard deviation of the associated drain current $\sigma(\Delta I_d/I_d)$ and $Y$ function $\sigma(\Delta Y/Y)$ mismatch vs gate voltage are shown in Fig. 21. These characteristics can be well fitted with the matching model
given in Eqs [10] and [11] and which accounts for 3 matching parameters i.e. $\sigma(\Delta V_t)$, $\sigma(\Delta \beta/\beta)$ and $\sigma(\Delta R_{sd})$ as [IOA 15],

$$
\sigma\left(\frac{\Delta I_d}{I_d}\right)^2 = \left(\frac{\sigma_m}{I_d}\right)^2 \sigma(\Delta V_t)^2 + (1 - G_d \cdot R_{sd})^2 \sigma(\Delta \beta/\beta)^2 + G_d^2 \sigma(\Delta R_{sd})^2
$$

[10]

and

$$
\sigma(\frac{\Delta Y}{Y})^2 = \frac{\beta \sigma(\Delta V_t)^2}{4 \beta n^2 (kT/q)^2} + \frac{1}{4} \sigma(\Delta \beta/\beta)^2
$$

[11]

where $G_d$ is the channel conductance and $\beta = WC_{ox} \mu_0 V_d/L$ is the gain factor. According to this model, it should be noted that the $Y$-function variability is dominated by the $V_t$ mismatch below threshold and then decreases to a plateau limited by the $\beta$ mismatch at strong inversion. This behavior is similar for the drain current variability except that there is an additional contribution of $R_{sd}$ mismatch above threshold, which tends to prevail for large $W/L$ ratios [IOA 15, IOA 16].

The corresponding area normalized matching parameters defined as $iA_{\Delta V_t} = \sigma(\Delta V_t) \sqrt{W/L}$ and $iA_{\Delta \beta/\beta} = \sigma(\Delta \beta/\beta) \sqrt{W/L}$ are given in Fig. 22 for various geometries and FDSOI technologies [IOA 16]. Overall, these values demonstrate that state-of-the-art variability performances are achieved for advanced FDSOI technologies.

Finally, Fig. 23 shows that the standard deviation of the series resistance mismatch $\sigma(\Delta R_{sd})$ varies typically as the reciprocal device width. As expected, the average value of $R_{sd}$ is also scaling as $\rho_{SD} W$ with $\rho_{SD} \approx 400 \ \Omega \ \mu$m for 14nm FDSOI technologies. This behavior shows that the normalized series resistance local variability $\sigma(\Delta R_{sd})/R_{sd}$ is nearly constant, around 15% within 1.5 times variation, as a function of width for this 14nm FDSOI technology in line with 28nm results [IOA 16].
This drain current matching characterization and modelling have been extended to all operation region of FDSOI MOS devices [KAR 17b]. In particular, the drain current mismatch model of Eq. [10] has been generalized to non linear operation region and to include subthreshold slope variability through ideality factor n variations [KAR 17b]:

\[
\sigma^2 \left( \frac{\Delta I}{I_D} \right) = \left( \frac{g_m}{I_D} \right)^2 \cdot \sigma^2 (\Delta V_f) \cdot \left[ 1 - \left( \frac{g_m + g_d}{g_m} \right) \cdot R_{SD} \right] + \sigma^2 (\Delta \beta / \beta) \cdot \left( \frac{g_m}{g_m + g_d} \right)^2 + \sigma^2 (\Delta R_{SD}) + \left[ \ln \frac{I_D}{I_D,th} \right]^2 + \left[ \exp \left( - \frac{I_D,th}{I_D} \right) - 1 \right]^2 \cdot \sigma^2 (\Delta \beta / \beta) \tag{12}
\]

This model enabled the fits of the drain current variance both as a function of gate voltage and drain voltage up to saturation region (see Fig. 24).
Figure 24. Experimental results (symbols) and model (lines) of $\sigma^2(\Delta \text{id/\text{id}})$ versus gate (a, b) and drain (c, d) voltage. After [KAR 17b].

6. Conclusions

We have reviewed the main electrical techniques to characterize the important MOS device parameters and illustrated them by typical results obtained on advanced FDSOI technologies. First, the capacitance-voltage measurements have been employed for the vertical stack characterization of FDSOI structures with HK/MG gate, ultra thin film channel, thin box oxide and back plane substrate. Then, the MOSFET parameter extraction methods have been illustrated, as well as the transport and mobility assessment using various techniques (I-V, magneto-transport). Finally, the methodology to study the local variability of the MOSFET electrical characteristics has been discussed.

References


