Tunnel FETs for ultra low Power Nanoscale Devices

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ABSTRACT. Future ICs are facing dramatic challenges in performance as well as static and dynamic power consumption, which could be overcome using disruptive concepts, device architectures, technologies and materials. Promising solutions includes III-V channels, heterojunctions, 2D layers, multi-gates structures, nanowires (NWs), tunnel FETs (TFETs), ferroelectric FETs (Fe-FETs), and hybrid devices. In the domain of small slope switches, which are very interesting for ultra low power operation, TFETs, Fe-FETs and hybrid devices seem very promising. Thus far, no one has experimentally demonstrated a TFET that has simultaneously both a CMOS-competitive driving current Ion and a sub-60 mV/decade subthreshold swing over several decades. But recently, substantial improvements of TFET and hybrid device performance have been reported, showing that these novel device architectures using new materials and carrier transport could be used for several applications.

KEYWORDS. Tunnel FET, Nanowire, III-V channel, 2D material, Multi-gate, Ferroelectric FET, Hybrid device, Heterojunction, Subthreshold swing.

1. Introduction

Many innovative technologies are needed for future More Moore and More than Moore Nanoelectronic applications in order to overcome the following limits: substantial increase of energy consumption and heating which can jeopardize future IC integration and performance, reduced performance due to limitation in traditional high conductivity metal/low k dielectric interconnects, limit of optical lithography, heterogeneous 3D integration of new functionalities for future sustainable, secure, ubiquitous and pervasive nanosystems, etc. [BAL 10, BAL 14].

With respect to the substantial reduction of the static and dynamic power consumption of future high performance/ultra low power terascale integration logic and autonomous nanosystems, new materials and novel device architectures are mandatory for NanoCMOS and Steep Slope Switch Nanoelectronics Devices, as well as new circuit design techniques, architectures and embedded softwares [BAL15].

The paper will focus on the main trends, challenges, limits and possible solutions for ultralow power and high performance nanoscale devices in the Beyond CMOS arena, including many novel materials, ultra-thin films, multi-gates, nanowires for small slope switches, in particular Tunnel FETs and Hybrid devices. These devices allow in particular to obtain a subthreshold slope, which represents the commutation between the OFF and ON states of the transfer characteristics, lower than 60mV/decade, which is the limit of traditional MOSFET operation at room temperature, and are thus promising for very low energy applications.

2. Basic principle of Tunneling devices

The basic operation of a Tunnel FET is shown in Figure 1. When the barrier between the conduction and valence bands controlled by the gate is thin enough, electrons can flow by tunnel effect between source, channel and drain of the TFET, allowing low inversion slopes below 60 mV / dec, which is the limit of CMOS devices at 300K. This behavior is of great interest for very low voltage / consumption circuits which represent the greatest challenge for future generations of nanoelectronic devices.

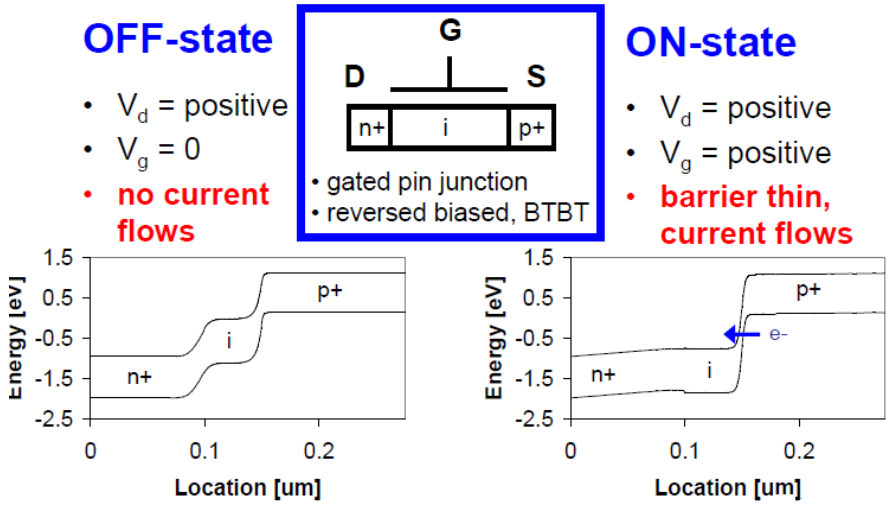

Figure 1. *Basic operation of a Tunnel Field Effect Transistor*

Figure 2 shows an example of a silicon TFET, with opposite doping sources and drain, whose performance in the ON state could be greatly improved using two gates, a thin Si film and a high permittivity dielectric.

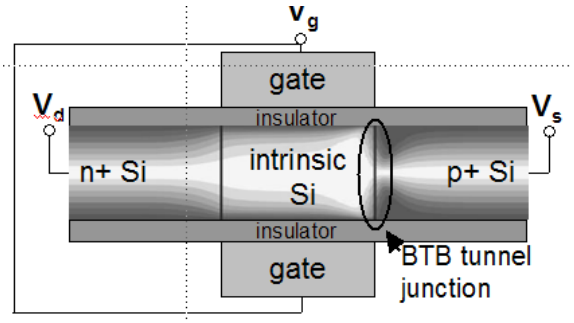

Figure 2. *TFET control by a double gate (front and buried gates)*

3. Tunnel FET with Si, Ge, III-V channels

Figure 3 shows a low experimental inversion slope for SOI FET Tunnel of about 40 mV / dec. The drain current at the ON state can moreover be improved by moving from a SOI TFET to a TFET on SiGe / OI, the best performances being obtained for a TFET Ge / OI with an increase of a factor greater than a thousand compared to SOI due to an effective mass and a reduced bandgap for Ge with respect to Si [MAY 08].

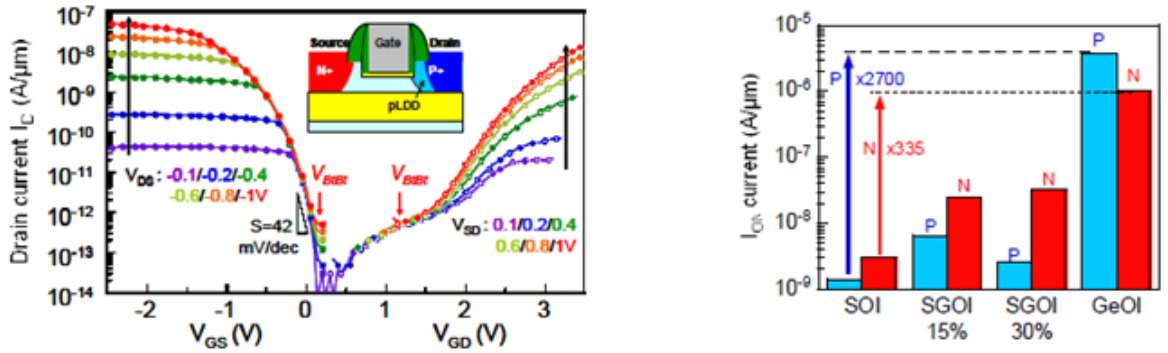

Figure 3. *(a) TFET SOI characteristics Id (Vg) of Lg = 100nm in p (left) and n (right) operation, with a silicon thickness tsi = 20nm showing a slope S of 42mV / dec; (b) ON current of n and p type TFETs with Lg = 400nm for SOI, SiGe / OI channels with different percentages of Ge, and GeOI (TGe = 60nm)*

Alternative to Si materials, Ge or III-V channels are not necessarily useful for MOSFET technologies, but can nevertheless find their full usefulness for tunneling FET components. TFETs made on III-V materials with low bandgap and low effective mass of electrons to boost the band-to-band tunneling effect on thin multigate films are promising with slopes down to 20 mV / decade obtained by quantum simulation for Nanowires [LUI 09].

The quantum simulation study of TFET Nanowires on InAs show that, as for MOSFETs, Nanowire diameters of less than 5 nm are necessary if we want to maintain good subthreshold slopes better than the MOSFET for sub-decananometer gate length (Fig. 4) [CON 11].

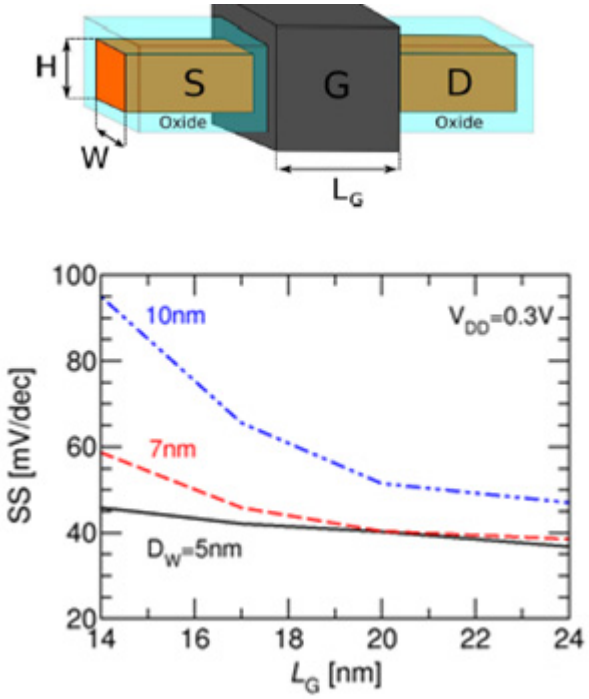

Figure 4. *Subthreshold slope as a function of the diameter of the Gate All Around InAs Nanowire and the gate length with a supply voltage Vdd = 0.3V*

Fig. 5 compares, by quantum numerical simulation, different architectures of TFET nanowires made on III-V materials with the silicon MOSFET architecture. The best performances are obtained for a quantum well TFET at the InAs-GaSb-InAs source, giving a slope of the order of 30 mV / dec and a drain current at the ON state of the order of 500 mA / µm [PAL 15]. However, the experimental performances are still very far from these promising results because the technologies have to face many challenges: integration of new III-V materials, innovative architectures of components, reduction of the densities of defects in order to eliminate the trap-assisted -tunneling that degrades the slope in weak inversion and the current in the ON state.

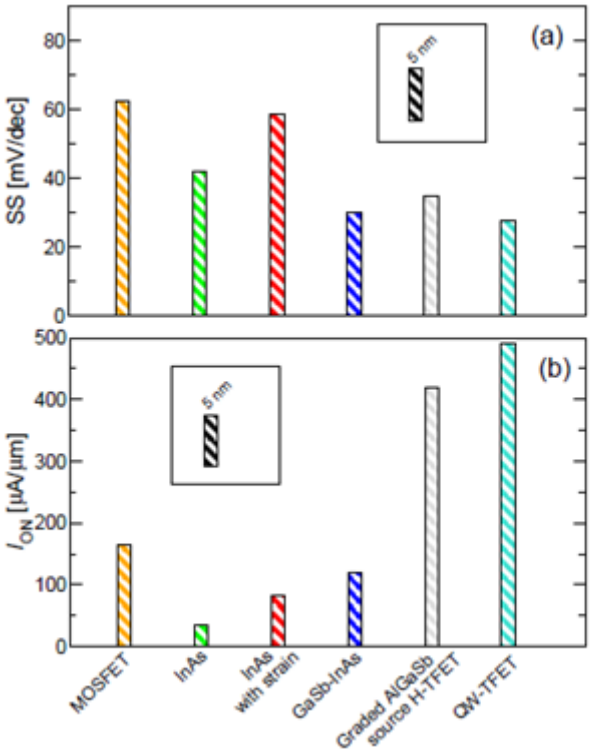

Figure 5. *Ion and subthreshold slope for different nanowire architectures (d = 5nm, Lg = 17nm, Ion at Ioff = 5nA / µm): MOSFET, TFET InAs, TFET InAs with strain, TFET with GaSb-InAs heterostructure, Graded AlGaSb Source Heterostructure TFET with a graded length of Tgrad = 5nm, Quantum Well InAs-GaSb-InAs TFET with Twell = 3nm*

4. TFET on 2D materials

The 2D materials represent the ultimate limit of reduction of the channel dimensions of the transistors inducing the best electrostatic. The first material of this type was graphene (semi-metal) but other 2D materials more suitable for logical applications (including a band gap) were then developed.

Figure 6 shows the integration limits of Tunnel FETs made on a 2D layer. Indeed, a TMD (Transition Metal Dichalchogenide) WTe2 channel double gate TFET shows a possible integration up to a 7nm gate length, with an excellent theoretical value of the ON state current obtained by quantum simulation. Below this value, a substantial degradation of the slope S is obtained, with a value that goes back above 60 mV / dec [JIA 15].

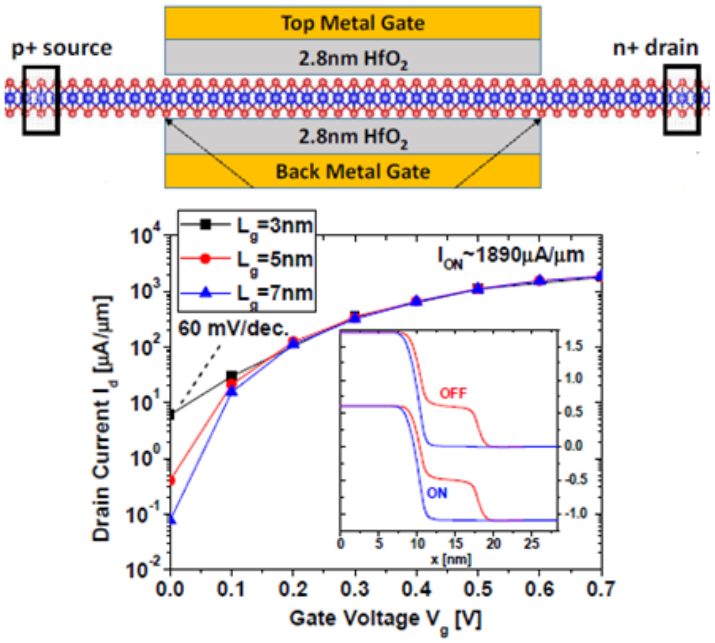

Figure 6. *TFET double gate on WTe2 layer with transfer characteristic Id (Vg) as a function of gate length (Vd = 0.5V, S / D doping $10^{13}cm^{-2}$)*

The comparison of homojunction and heterojunction 2D TFET by quantum simulation is shown in Fig. 7. The WTe2-MoS2 heterojunction leads to a better driving current Id than the homojunction MoS2 TFET, and a better ON current compared with MoS2 MOSFET for a gate bias lower than 0.4V [CAO 15], showing the substantial interest of these devices for ultra low power operation.

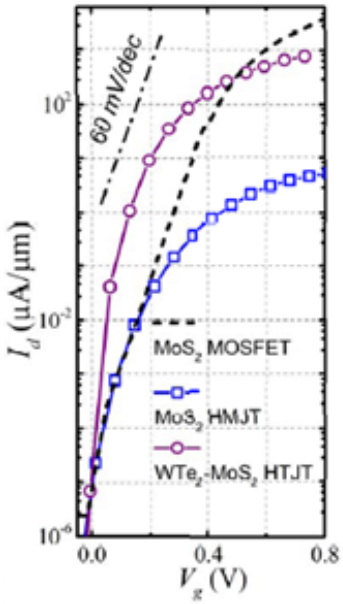

Figure 7. *Id-Vg transfer characteristics for homojunctions MoS2 and heterojunction WT2-MoS2 TFET compared with MoS2 MOSFET, Vd=0.5V, Lg=12nm*

A vertical InAs/GaAsSb/GaSb Nanowire TFET has recently shown a significant improvement of the driving current (Fig. 8a). Indeed, the $I_{60,}$ which is the maximum current for which a sub-60mV/dec subthreshold slope is obtained, is 0.056 μA/μm at Vds=0.1V (Fig. 8b), and 0.31 μA/μm at Vd=0.3V, which represents a factor about 30 improvement compared with previous experimental results. The minimum swing is 50mV/dec at 300K [MEM 16].

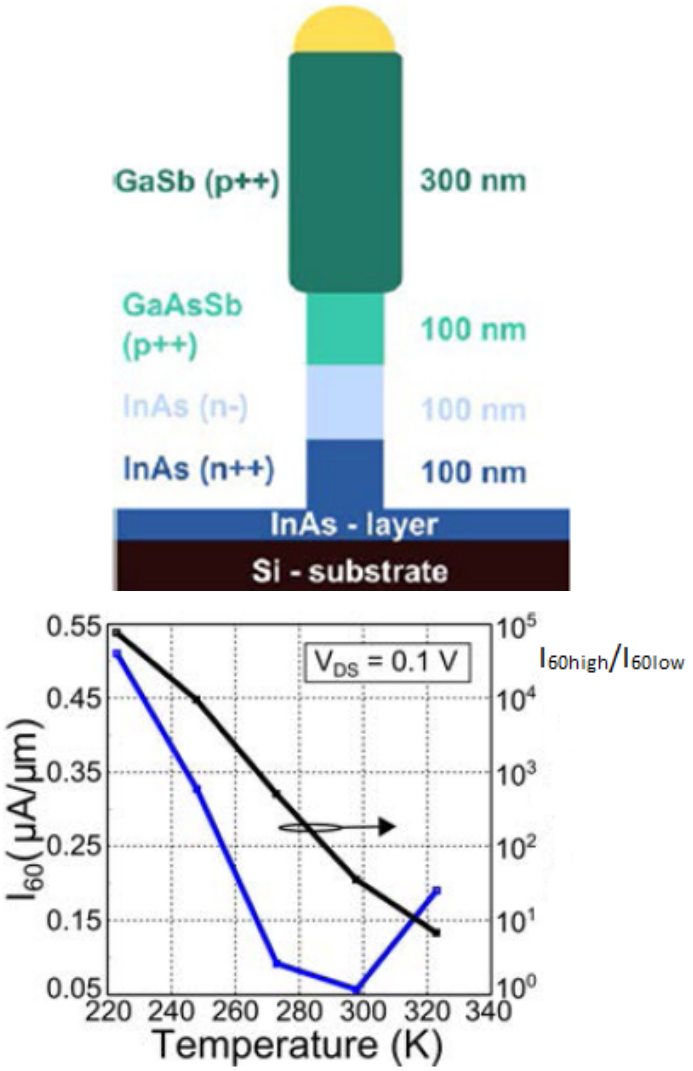

Figure 8. *(a) Vertical InAs/GaAsSb/GaSb Nanowire TFET and (b) I60 and the ratio I60high / I60low (ratio between the highest and lowest current for the sub-60m/dec region) as a function of temperature, Vd=0.1V, NW diameter d=20nm, Lg=100nm*

5. Hybrid devices:

5.1. *Ferroelectric Tunnel FET*

Since it is currently difficult to obtain good experimental performance in drain current at the ON state of Tunnel FETs, an interesting option is to combine the tunnel transport between source and drain with a gate using a ferroelectric material inducing a negative capacitance of the MOS structure and leading to an amplification of the gate bias. This combination significantly improves the subthreshold slope, the drain current and the transconductance compared to the TFET alone with a traditional gate (Fig. 9) [LEE 13].

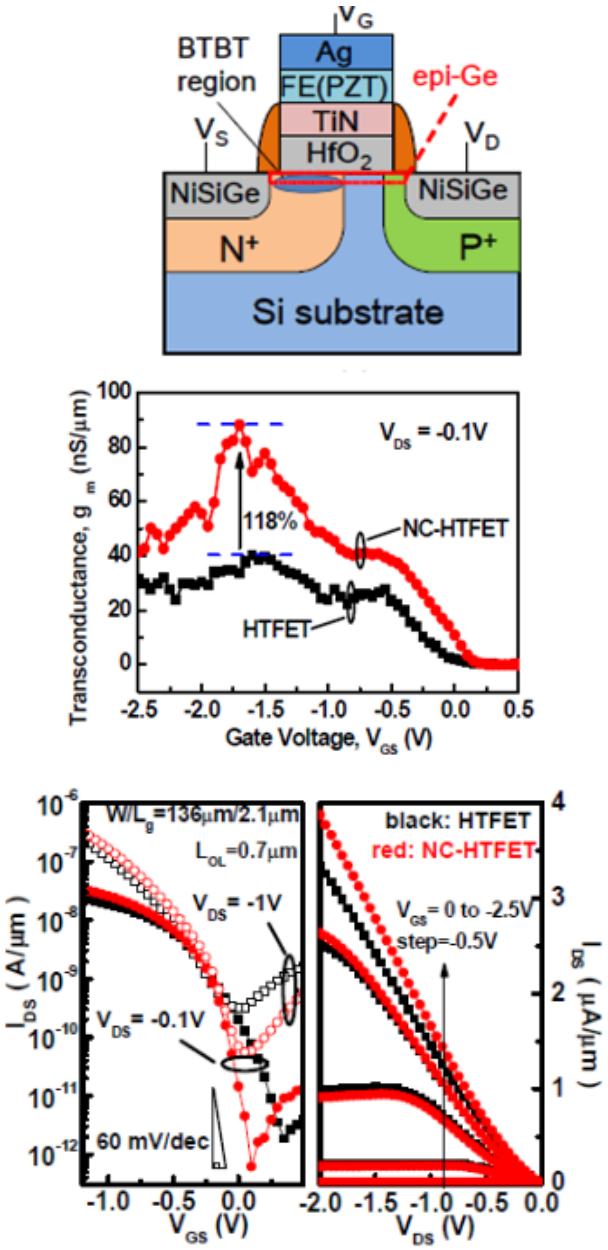

Figure 9. *(a) Hybrid device FeTFET combining a tunneling transport between source and drain tunneling (TFET) and a ferroelectric gate (PZT) for improving the subthreshold slope (c), the drain current (c) at the ON state and the transconductance (b)*

5.2. *Phase Change TFET*

A more original version of the Small Slope Switches components has recently been proposed by combining a phase change material in the gate (VO2) whose insulator-metal transition is induced by an electric excitation by polarizing the gate, and a tunnel transport in the channel. A slope of about 4mV / dec over several decades is observed for voltages not too low close to 1V (Fig. 10) [CAS 16].

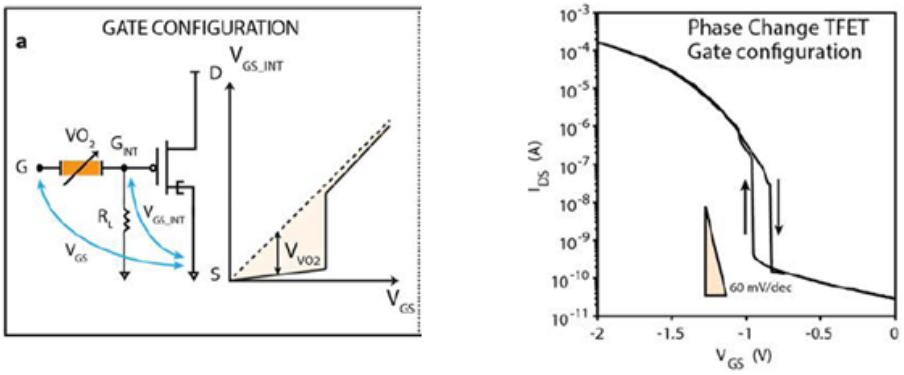

Figure 10. *(a) FET tunnel with phase change VO2 gate showing an insulator-metal transition by electrical excitation with very good subthreshold swing*

6. Nanoscale devices Roadmap

Figure 11 presents the comparison of the theoretical subthreshold swing for the most advanced nanoscale FET architectures and materials of the literature as the function of the gate length. The ITRS (International Technology Roadmap for Semiconductors) and IRDS (new International Roadmap for Devices and Systems) needs for logic devices are also shown vs time horizons. The best performance for the swing of CMOS devices at the end of the Roadmap close to 60mV/decade obtained for Multi-gate (Omega Gate in the figure) Nanowire FET with very small wire diameter (3nm) and Double Gate MOSFET with TMD (Transition Metal Dichalcogenide) channel (MoS2 in the figure) channel. However, at the end of the next decade, sub-60mV/decade swing is needed, which can only be obtained with small slope switches (Tunnel FET with III-V or 2D channels in the figure).

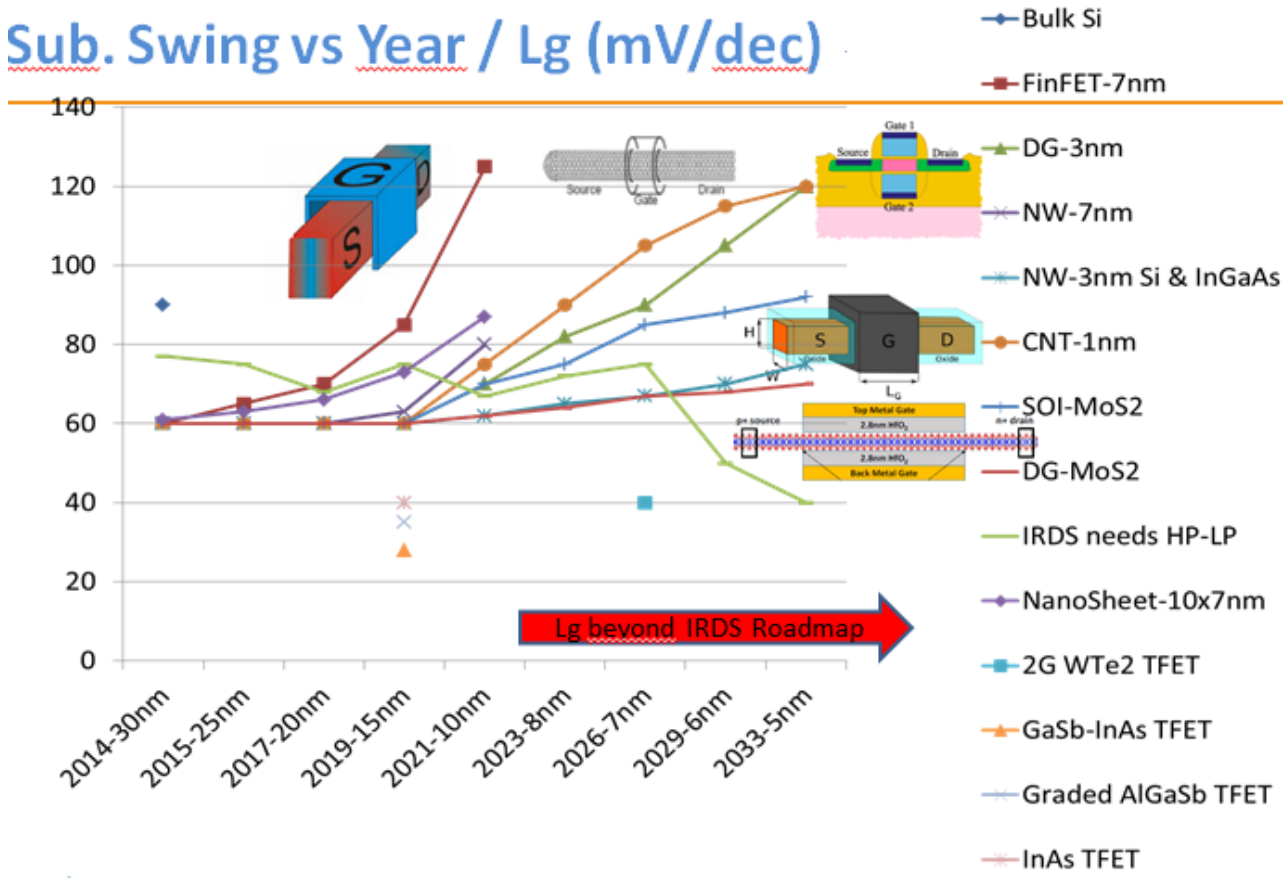

Figure 11. *Advanced simulations of subthreshold swing (mV/dec) vs. gate length and time horizon for various device architectures (Bulk Si, FinFET, Double Gate, Nanowire with various diameters, Carbon NanoTube, MOSFET on Insulator, Nanosheet) and channel materials (Si, InGaAs, InAs, Heterojunction GaSb-InAs, Graded AlGaSb, MoS2, WTe2), compared with IRDS needs*

7. Conclusion

Small slope switches are very interesting specially for ultra low power operation. TFETs, Fe-FETs and Hybrid devices seem particular promising. Recently, substantial improvements of TFET and Hybrid device performance have been reported, showing that these novel device architectures using new materials and carrier transport could be used for several future applications requiring very low energy consumption or autonomy, for instance in the field of IoT ambient devices. These novel device architectures, using multi-gate, high dielectrics, ultra thin channels, combined with advanced materials, e.g. Ge, III-V, 2D, Heterogeneous, Ferroelectric or Phase-Change, could lead to interesting performances that could overcome some of the CMOS limitations in the future.

8. Acknowledgements

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