

Capturing Performance Limiting Effects in Tunnel-FETs

A Device Re-Evaluation Résumé

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ABSTRACT. In this paper a two-dimensional analytical Tunnel-FET model is revised. It is used to evaluate performance enhancing measures for the TFET regarding device geometry and physical effects. The usage of hetero-junctions is discussed and a way to suppress the ambipolar behavior of the TFET is shown. In focus of this work are the emerging variability issues with this new type of device. Random-dopant-fluctuations (rdf) have a major influence on the device performance. This effect is analyzed and compared with rdf effects in a MOSFET device. The drawn conclusions lead to a re-evaluation of performance limiting aspects of fabricated TFET devices.

KEYWORDS. Random Dopant Fluctuation (RDF), Randomized Profiles, Gaussian Doping Profiles, Trap-Assisted-Tunneling (TAT), Double-Gate (DG) Tunnel-FET, Analytical Modeling.

Introduction

« The focus of this paper belays on one of the most promising devices to continuously overcome the 60 mv/dec slope limitation of MOSFETs, and with that, be its successor for at least low power applications. Based on its band-to-band (b2b) tunneling current transport mechanism in the on-state, the tunneling field-effect transistor (TFET) provides this possibility [Seabaugh et al., 2016]. The biggest challenge so far with these new devices is the trade-off between a steep subthreshold slope and a sufficient on-current. Nowadays the full potential of technological possibilities is used for fabricating TFETs : From conventional to III-V semiconductors, hetero-structures, straining techniques, high- κ gate insulators and a wide range of different 2D and 3D structures are investigated. So far a specific selection regarding material combination and structure has not been made, although the greatest potential show 3D structures using III-V semiconductors and high- κ gate dielectrics [Seabaugh et al., 2016].

1. Device Overview

The device geometry for the model derivation has to be, on one hand, adaptable to different geometries and on the other hand kept plane to simplify the calculations. For this work the DG structure in figure 1a) is chosen. It is more complex than the basic single-gate bulk device and it can be adapted to cover even Fin-structures, making it a perfect compromise between geometric complexity and mathematical simplicity. Source and drain region have a length of l_{sd} , the channel region length is l_{ch} and their thickness is t_{ch} . The high- κ insulator consists of HfO_2 and has a thickness of t_{in} . The width of the device is defined as w . The TFET is basically a gated p-i-n diode. An electron on-state current occurs for an n-type device (figure 1a)). The source is highly p-doped, the channel stays intrinsic and the drain has a reduced n-doping. The most simplest homo-junction devices only contain silicon as semiconductor material in

source, channel and drain region. However, the possibilities of different material combinations to create hetero-junction TFETs are versatile [Seabaugh et al., 2016]. These alternative materials, mostly III-V semiconductors, provide high carrier mobilities and small direct band-gaps, which enhance the tunnel effect, and with that, device performance. The gate insulator material has a major influence as well. Thereby, the permittivity of the insulator ϵ_{in} directly correlates to its ability to improve the electrostatic influence of the gate electrode on the channel region. The usage of high- κ gate insulators, like HfO_2 , serves as a common tool for performance enhancement. Figure 1b) shows the different states of the device with their predominant currents.

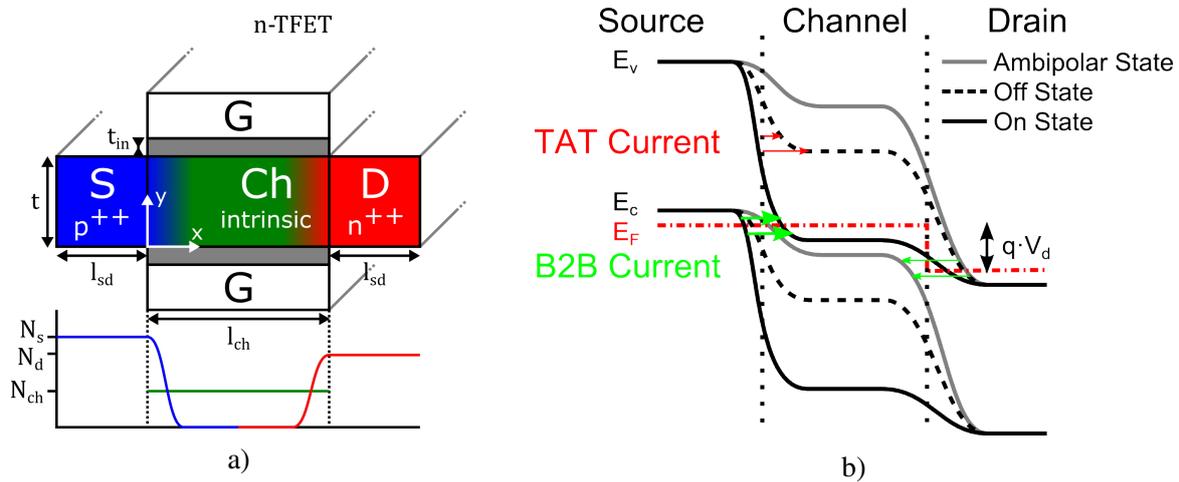


Figure 1. a) Schematic geometry of an n-type DG Tunnel-FET, showing its structural parameters and doping profiles. b) Schematic band structure of a n-Tunnel-FET showing the different operating regimes and their dominating currents.

In the on-state the band-to-band (b2b) current at the source-to-channel junction is dominating, whereby in the off-state the trap-assisted-tunneling (tat) current is predominant. In the ambipolar-state a reduced b2b current at the drain/channel junction is present. The reduced drain doping results in an increased tunneling distance at the drain/channel junction (see Fig. 1b)), which suppresses the current. The influence of random dopant fluctuations (rdf) on device performance is increasing for the ongoing scaling of nanoscale transistor devices. In the current MOSFET technology this effect mainly affects the threshold voltage, which is reduced in terms of the actual distribution of single dopants within the channel region [Shin et al., 2009]. These dopants are the result of a diffusion process, that occurs during the annealing step in the fabrication of the doped source/drain region. This effect influences the TFETs as well and its effect on device performance has to be investigated. The schematic influences of rdf on the drain current in TFETs are illustrated in figure 2. The discretization of dopants leads to different current characteristics. Thereby, the standard deviation of the current can directly be calculated with the current level leading to σ_{I_d} . An equivalent range in gate voltage can also be calculated to cover this current variation, which leads to σ_{V_g} .

2. 2D Analytical Model Review

The calculations of the tunneling probability and device current of the TFET require an accurate solution of the potential and electric field, not only within the channel region of the device, but also in the source and drain extensions. This electrostatic solution was firstly introduced in [Graef et al., 2014b]. For a high on-current an abrupt doping profile at the source tunneling barrier is necessary but technologically

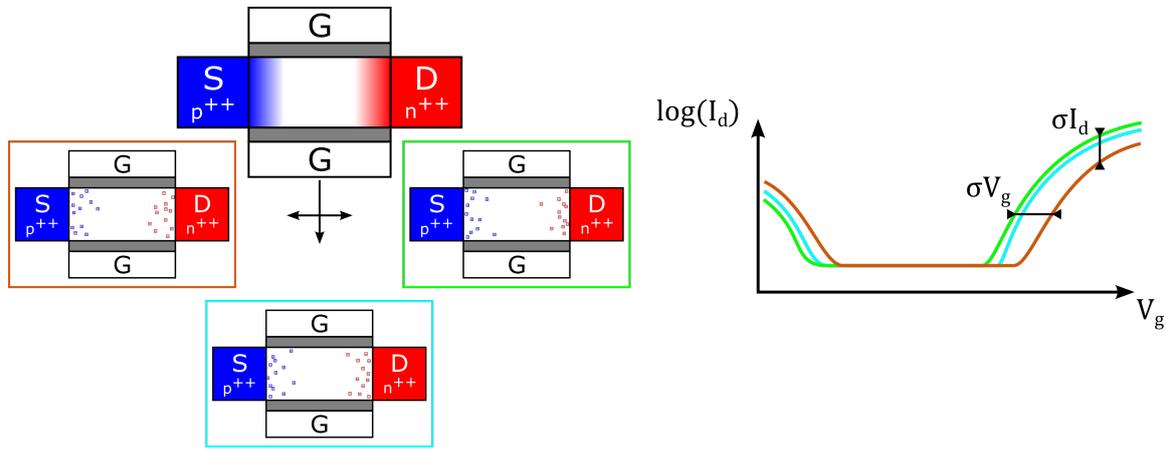


Figure 2. Random dopant fluctuation influence on TFET device current, showing standard deviation for gate voltage σ_{V_g} and the standard deviation of the drain current σ_{I_d} .

difficult to achieve. Therefore, a model firstly introduced in [Graef et al., 2015] is implemented, which captures the impact of the doping profile steepness on the electrostatics and hence, the device current. The band-structure of the device is needed to properly calculate the tunneling probability and hence, the device current. Especially for hetero-junction devices it is important to consider the band structure, since here kinks may occur due to different material dependent parameters. The closed form calculations of the electric field are based on the single-vertex approach firstly introduced in [Graef et al., 2014a], which leads to an expression for the electric field based on non-constant boundary potentials. Two different tunneling mechanisms are present in the TFET. Direct tunneling is possible in the region, where the bands overlap and a tunneling through the forbidden region occurs. Here also a trap-assisted tunneling is possible for carriers with the same energy level as the trap. They can emit into the trap and subsequently tunnel onto the right-hand band. There are four different tunneling events occurring in all different states of the TFET. Figure 3 illustrates the predominant tunneling events for each state and indicates the omnipresence in the resulting current transfer characteristics. In the on-state the band-to-band tunneling at the source/channel interface prevails T_{b2b}^s . In the transition from on- to off-state, the trap-assisted-tunneling at the source side increases T_{tat}^s , which is then overtaken by the tat at the drain side T_{tat}^d in the transition from off- to the ambipolar-state. The band-to-band tunneling at the drain side T_{b2b}^d is predominant in the ambipolar-state.

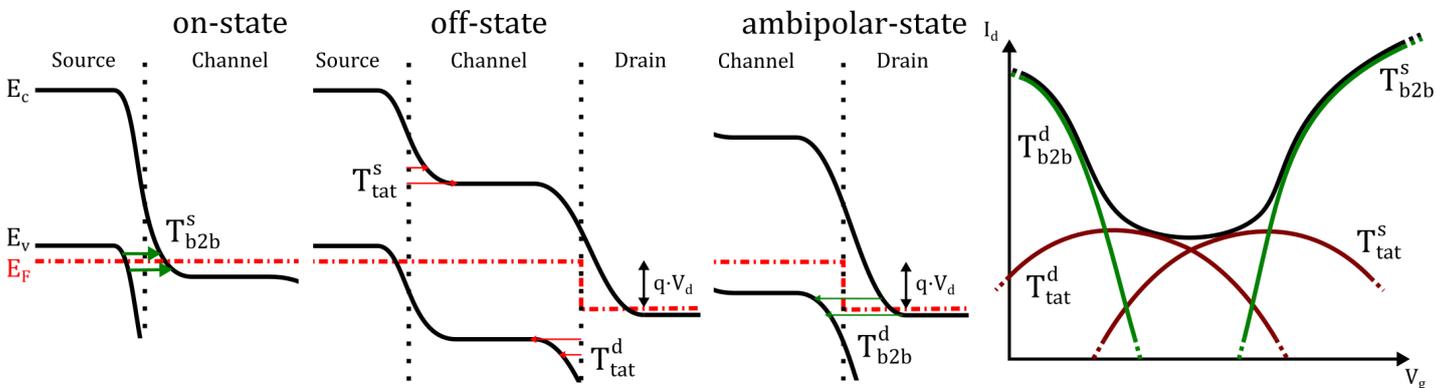


Figure 3. Predominant tunneling events in the three states of the TFET. T_{b2b}^s in on-state, $T_{tat}^{s/d}$ in off-state and T_{b2b}^d in ambipolar state. The omnipresence of all events is indicated in the resulting current transfer characteristics.

The WKB approximation is used as a method for estimating a tunneling probability through a rectangular barrier. For the calculation of the tunneling probability for all different tunneling events, a general

quasi 2D WKB approach is introduced in [Graef et al., 2014a]. By considering a tunneling path from a point in source region to a point on the same energy level in channel region (see Fig. 4a)), a triangular barrier can be defined with the help of the electric field (potential slope). Within the TFET, the traps are located at the source/channel and drain/channel junction of the device [Vandooren et al., 2013]. Figure 4b) schematically shows the exponential trap distribution N_T at the source/channel interface. The probability of tat is calculated the same way as the b2b tunneling probability [Graef et al., 2014a].

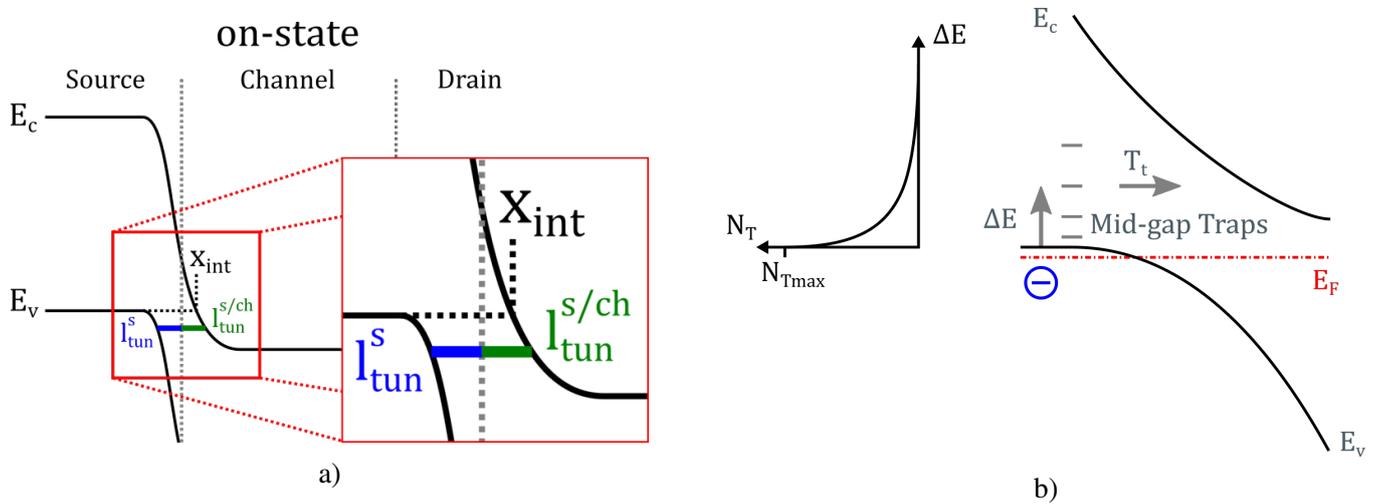


Figure 4. a) B2b tunneling length in on-state at source/channel junction. b) Tat tunneling at the source/channel junction, showing the exponential trap distribution N_T .

The last part of the analytical model consists of the device current calculation, which is based on Landauer's transmission theory [Gnani et al., 2012]. In order to determine the carrier concentration on both sides of the barrier, the Fermi-statistics are needed (see Figure 5). With the Fermi-statistics in both regions, a drain bias depending carrier probability gradient is given, which is used for the final current calculation firstly introduced in [Graef et al., 2014a].

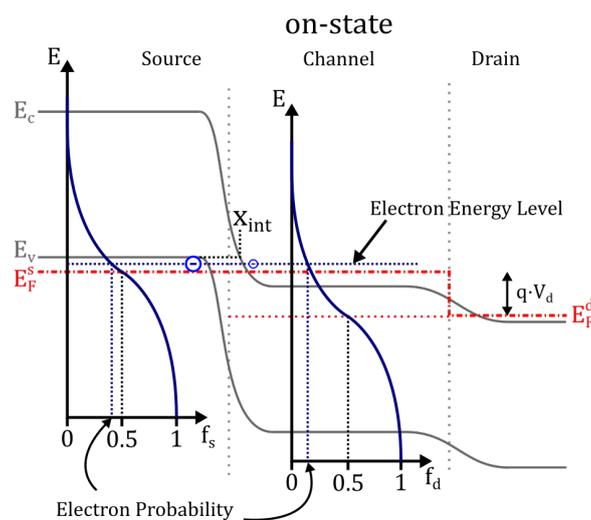


Figure 5. b2b current calculation based on Landauer's transmission theory, showing source- and drain-related Fermi-statistics $f_{s/d}$.

3. DC Performance Evaluation

In this section, the model is verified by comparing to TCAD Sentaurus simulation data. Therefore, a standard device and the simulation setup is specified. The standard device parameters for the comparison to TCAD simulation data are specified in table 3.1. Investigated is a silicon double-gate n-TFET with a high- κ HfO_2 gate insulator to maximize the gate control over the channel region.

Parameter	Value	Parameter	Value
l_{ch}	22 nm	N_s	10^{20} cm^{-3}
t_{ch}	10 nm	N_d	10^{20} cm^{-3}
t_{in}	2 nm	N_{Tmax}	$10^{12} \text{ eV}^{-1} \text{ cm}^{-2}$
l_{sd}	20 nm	Device material	Si
σ	1 nm	Oxide material	HfO_2

Tableau 3.1. Standard TCAD simulation setup for model verification.

In the first results two significant performance limiting aspects are investigated. As mentioned before, the device's off-state current is based on trap-assisted-tunneling events at the source- and drain/channel interface. Hereby, the current level directly correlates with the maximum trap concentration at these junction. The following results in figure 6a) show the influence of the maximum trap concentration on the off-state current for $N_{Tmax} = 10^{12}, 10^{13}, 10^{14}, 10^{15}, 10^{16} \text{ eV}^{-1} \text{ cm}^{-2}$. The simulation results show a linear correlation between the trap concentration and the off-state current, which is correctly reproduced by the analytical model. This shows, that a low off-state current can be directly linked with a low trap concentration. Due to an improving subthreshold slope of the b2b-related current at low current levels, the off-state current level limits the lowest achievable subthreshold slope as well. Concluding from this behavior, the trap concentration limits the off-state current and has the highest influence on the minimum subthreshold slope. The second performance limiting aspect is the quality of the doping profiles at the channel interfaces. The steeper this profile, the steeper the bands in the channel region, and with that, the shorter the tunneling distances. By considering a Gaussian-shaped doping profile at the source/channel interface, the standard deviation σ of this profile is a measure of its quality. The results in figure 6b) show a comparison of the current transfer characteristics of the model with the simulation data for various standard deviation $\sigma = 0$ to 2 nm in 0.5 nm steps.

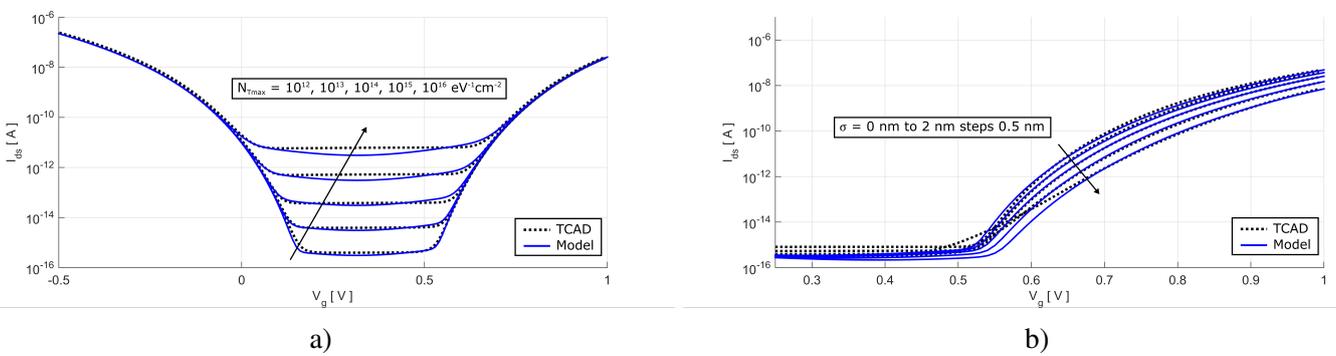


Figure 6. a) Influence of the maximum trap concentration on the TFET's off-state current for $N_{Tmax} = 10^{12}, 10^{13}, 10^{14}, 10^{15}, 10^{16} \text{ eV}^{-1} \text{ cm}^{-2}$ at $V_d = 0.7 \text{ V}$. b) Influence of the doping profile quality (standard deviation) at the source/channel junction on the device current for $\sigma = 0$ to 2 nm in 0.5 nm steps and $V_d = 0.7 \text{ V}$.

The doping profile based potential extension is able to predict the worsening of the subthreshold slope

and on-state current correctly for $\sigma = 0.5, 1 \text{ nm}$. For more extended profiles only the reduction in on-state current is captured well. The ambipolar behavior of the TFET occurs because of its asymmetrical doping. It leads to additional complexity in circuit design and should be avoided if possible [Hraziia et al., 2012]. The simplest way, which can easily be captured with the analytical model, is a reduction of the drain doping concentration. Such a measure has direct influence on the band steepness at the drain/channel junction, which can be equated with an increase of tunneling distance leading to a significant current reduction. A high variation of the drain doping can not be captured by the model with the fitting for the standard device, hence all drain doping variations have to be fitted separately. In figure 7a) the influence of the drain doping concentration on the ambipolar-state current is illustrated for $N_d = 10^{20}, 5 \cdot 10^{19}, 10^{19}, 5 \cdot 10^{18} \text{ cm}^{-3}$. The model shows a good fit with the TCAD simulation data. There are several advantages III/V semiconductors offer compared to standard silicon. Their improved physical parameters such as carrier masses and mobilities directly enhance device performance. If they are used to form hetero-junctions, their smaller band gaps are beneficial for shorter tunneling distances, which results in increased currents [Seabaugh and Zhang, 2010]. To give a comparable example, the standard device is used with different source materials to generate a hetero-junction at the source/channel interface. The investigated materials are : germanium (Ge), a silicon germanium alloy ($\text{Si}_{0.5}\text{Ge}_{0.5}$) and the standard Si TFET for comparison. The analytical model has to be fitted individually for each hetero-junction. The results in figure 7b) show the influence of two different hetero-junctions on the current transfer characteristics. The model is able to calculate the current with high accuracy. Compared to the silicon TFET, both hetero-junction devices show an increase in on-state current, due to superior carrier properties. There is an improvement in subthreshold slope observable as well for the SiGe hj device. However, this beneficial effect disappears for the Ge hj entirely and the slope ends up even worse than in the Si TFET. This shows that hetero-junction engineering is quite delicate and has to be carried out thoughtfully. One important thing can be concluded from this comparison and the several fabricated hetero-junctions listed in [Seabaugh et al., 2016]. There seems to be a trade-off between the maximum on-state current and minimum achievable subthreshold slope. A higher current by hetero-junction could worsen the slope. Nevertheless, an optimum can be found where the positive influence of the hj benefits both, the current and the slope, like for the SiGe hj in figure 7b).

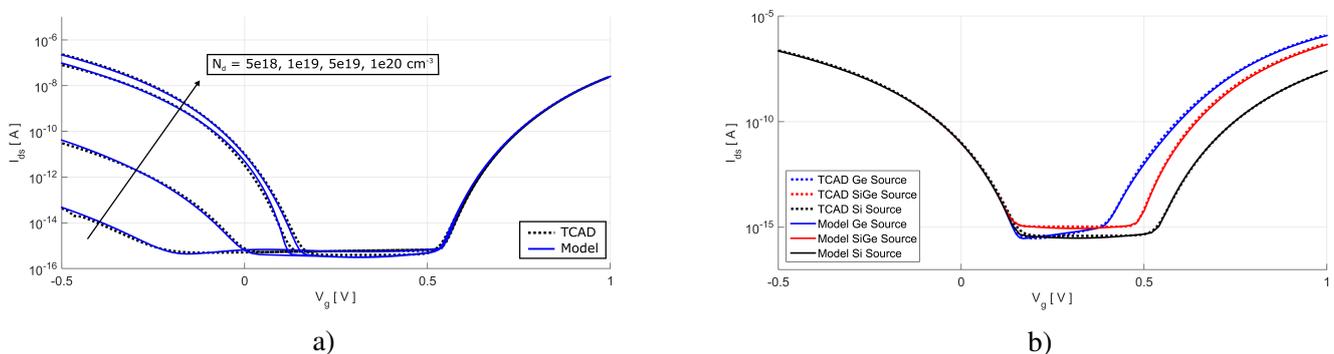


Figure 7. a) Influence of the drain doping concentration on the current in ambipolar-state of the TFET for $N_d = 10^{20}, 5 \cdot 10^{19}, 10^{19}, 5 \cdot 10^{18} \text{ cm}^{-3}$ at $V_d = 0.7 \text{ V}$. b) Influence of hetero-junctions within the TFET on the on-state current and subthreshold slope with a Ge/Si and $\text{Si}_{0.5}\text{Ge}_{0.5}$ /Si hetero-structure. Silicon device for comparison at $V_d = 0.7 \text{ V}$.

4. Variability Issues

In this section a comparative numerical rdf analysis for MOSFETs and TFETs is done in order to demonstrate the influence of this effect for different device types. The aim is to show general dependencies and give recommendations to improve device performance. To compare MOSFET and TFET in a reasonable way, the device geometry shown in figure 1a) is used for both devices. A silicon DG-n-TFET and a silicon DG-n-MOSFET are under investigation. The TFET device parameters are given in table 3.1. In the MOSFET the only differences are an n-type source doping and a p-type doped channel. To reduce the rdf effects of the channel doping in the MOSFET the doping concentration is kept low at $N_{ch} = 10^{15} \text{ cm}^{-3}$. Gaussian shaped doping profiles are applied at the channel junctions with different standard deviations $\sigma = 1, 1.5, 2, 2.5, 3 \text{ nm}$. The doping profile is randomized using the Sano method described in [Sano et al., 2002] with a cut-off parameter $k_c = 112.336 \cdot 10^6 \text{ cm}^{-1}$. This is done for a specific number of samples N .

4.1. RDF in MOSFETs

One of the main effects observed is a current shift, which can be expressed as a negative shift in threshold voltage [Shin et al., 2009]. Figure 8a) shows $N = 40$ current transfer characteristics simulated with randomized profiles. The mentioned threshold voltage shift in figure 8a) is clearly visible but the origin of this behavior can not be determined. In order to understand the rdf dependency in the MOSFET, figure 8b) shows the band structure of the device directly below the gate oxide for randomly chosen $N = 5$ devices. Generally, the band structures vary in energy due to the randomized doping level, which

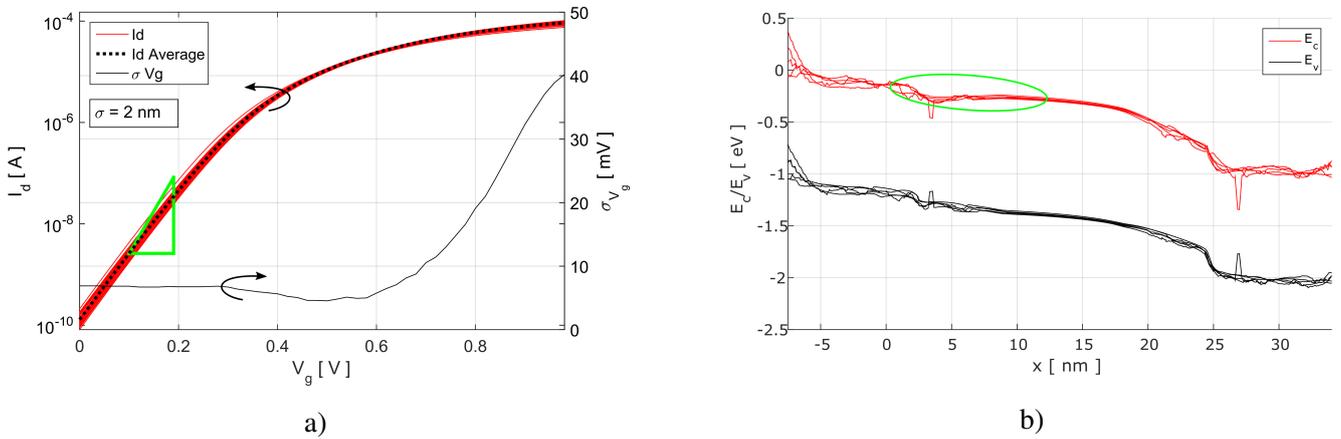


Figure 8. a) Current transfer characteristics of $N = 40$ dg-n-MOSFETs with randomized profiles, showing the calculated average current $I_{d,Avr}$ and standard deviation of the gate voltage σ_{V_g} at $V_d = 1 \text{ V}$. The green triangle indicates a 60 mV/dec slope. b) Band structure below the gate oxide at a randomly chosen cross-section for $N_{sample} = 5$ MOSFET devices in ON-state with $V_g = 1 \text{ V}$, $V_d = 1 \text{ V}$ and a standard deviation of the doping profile of $\sigma = 2 \text{ nm}$. The green circle shows the area of interest.

leads to a rippling band gap narrowing effect. These variations are also present at the energy barrier in the channel region of the MOSFET. Since the energy barrier is the current limiting parameter for the MOSFET (and its threshold voltage), a variation at the barrier directly leads to a varying current, which in the transfer characteristics is visible as threshold voltage variation. This connection is the reason for the rdf dependency. In a previous work [Graef et al., 2017] a method is developed for an rdf estimation in short-channel double-gate MOSFET devices. For MOSFETs, the current limiting attribute is the potential

barrier within the channel region. Therefore, only the influence of randomly distributed dopants within the channel region on the height of the potential barrier is important. This calculation is inspired by the impedance field method [Wettstein et al., 2003], where for each point of the device, RDF is described by the second-order statistical moments of the dopant distribution.

4.2. RDF in TFETs

The TFET simulation analysis in this section should give a deeper insight on the variability problems with this new device, since the alternative current transport mechanism shows completely different weaknesses regarding doping discretization and fabrication tolerances. The simulations are done using randomized profiles with the FEM-Simulator TCAD Sentaurus. Figure 9a) shows the current transfer characteristics for $N = 20$ samples with $\sigma = 1.5 \text{ nm}$. In comparison to the homogeneous doping profile, the threshold voltage of all samples is smaller and the S is worsening. In order to understand these effects, two samples are further analyzed. One with the best subthreshold slope S_{min} , and one with the worst S_{max} . Figure 9b) shows the current transfer characteristics of these two devices.

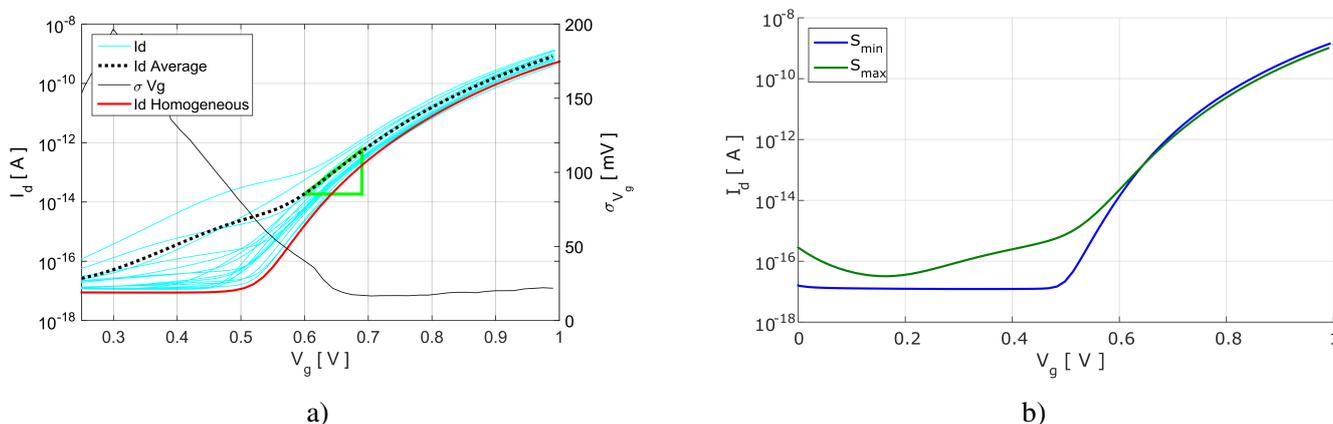


Figure 9. a) TFET drain current I_d for $N = 20$ randomized samples in comparison to a homogeneous doping profile. Standard deviation of the gate Voltage σ_{V_g} on the right. Green triangle = 60 mV/dec slope. b) Drain current of two devices with S_{min} and S_{max} .

A deeper insight on why the current characteristics are so different for the same device parameters, gives the band structure. In figure 10a) the band structure at the source/channel interface at characteristic gate voltages $V_g = 0.25, 0.5, 0.65, 1 \text{ V}$ is shown. The results are extracted at a position directly below the gate oxide where the maximum current of the device is flowing. At $V_g = 0.25 \text{ V}$ current flow starts in the S_{max} device, whereas in the S_{min} device this happens for a higher gate bias of $V_g = 0.5 \text{ V}$. At $V_g = 0.65 \text{ V}$ the current reaches the same level in both devices, and at $V_g = 1 \text{ V}$ the current in the S_{min} device is higher. The results in figure 10a) show that the threshold voltage of randomized devices is lower due to different distinctive band-gap narrowing effects near the channel junction. This greatly affects the gate voltage needed to get an overlap of the valence band in the source region with the conduction band in the channel. The subthreshold slope is decisively depending on the tunneling distance reduction rate for increasing V_g . For $V_g = 1 \text{ V}$ the tunneling distance of the S_{min} device gets shorter than for the S_{max} device at the same bias. This explains the reduced on-state current of the S_{max} device. Therefore, a discrete dopant located in the channel region near the junction is also negatively affecting the subthreshold slope of the device. A direct influence of the doping profiles standard deviation on σ_{V_g} is suspected. Meaning that, the fewer dopants are in the channel region, where charges are tunneling to,

the less deviation of the current is to be expected. Figure 10b) is supporting this suspicion and it shows a decreasing σ_{V_g} for less standard deviation of the doping profile.

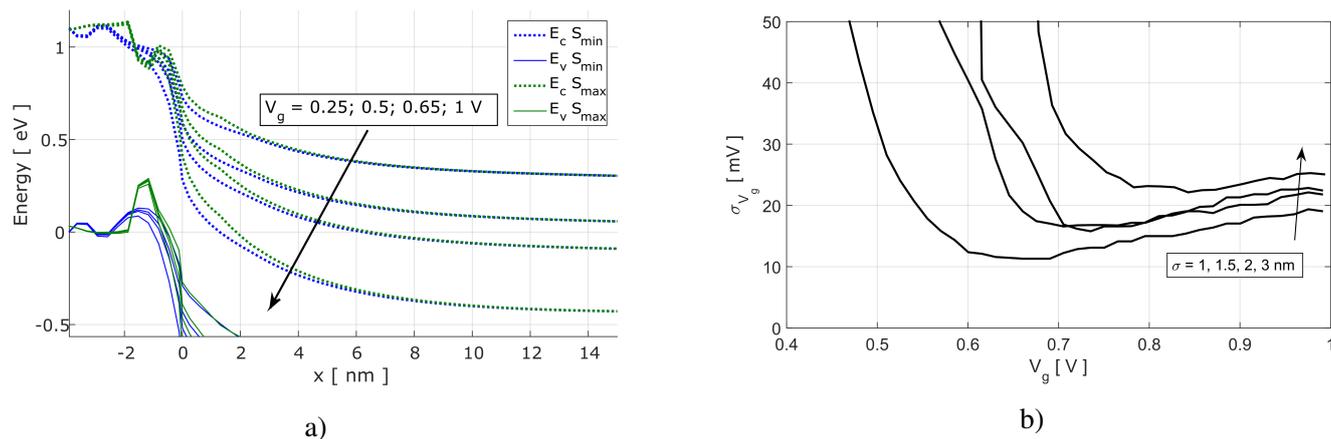


Figure 10. a) Band structure of two TFET devices with S_{min} and S_{max} at maximum current and characteristic gate voltages. b) Comparison of the gate voltage deviation σ_{V_g} for different doping profile standard deviations $\sigma = 1, 1.5, 2, 3 \text{ nm}$ at $N = 20$ and $V_d = 1 \text{ V}$.

The results of this simulation analysis provide an alternative explanation and understanding of the commonly known effects of threshold voltage shifting, subthreshold slope degradation and drain current variability in fabricated TFET devices.

5. Conclusion

In this paper a 2D analytical model for DG-n-Tunnel-FETs is revised. The focus lays on the fabrication-oriented difficulties such as doping profiles, occurring midgap traps and their influence on the performance. A reduced drain doping is used to reduce the ambipolar behavior of the device. It has been determined that the doping profile is mainly influencing the maximum on-state current. The trap-assisted tunneling current is predominant in the off-state of the device and has a major influence on the subthreshold slope. It has been shown that using hetero-junctions within the device can increase the performance if applied correctly due to the superior physical parameters. Rdf dependencies are investigated in MOSFET and TFET devices, the MOSFET current varies less compared to a TFET device. In the MOSFET rdf only has a direct influence on the potential barrier, which limits the device current. In TFETs, however, a variation of the potential near the channel junctions leads to more complex variations in tunneling distance and band-overlap position, and with that, a higher variation in device current. Optimization possibilities are steep doping profiles at the channel junctions, as well as low channel doping concentrations regardless of the device type. This work is giving an alternative explanation for fabricated device variability and performance limitations, which should be considered for future device evaluations.

Acknowledgments

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