Simulation of 2D material-based tunnel field-effect transistors: planar *vs*. vertical architectures

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ABSTRACT. Thanks to their thinness, self-passivated surface and large variety, two-dimensional materials have attracted much interest for their possible application in nanoelectronics. In particular, semiconducting transition metal dichalcogenides and their van der Waals heterostructures are very promising for the realization of low-power tunnel field-effect transistors. By means of self-consistent quantum transport simulations, we explore the performances of two alternative architectures for the devices: the planar architecture and the vertical architecture. While for the former, which is based on a *p-i-n* junction, the tunneling occurs laterally within the same two-dimensional material layer, in the latter the tunneling occurs through the vertical heterostructure between two different materials, which are chosen to have a convenient band alignment. Our results enable a comparison of the performance of two architectures in the ideal case, and can serve as a first guide for the choice of the transistor design based on the desired application.

KEYWORDS. tunnel field-effect transistor, 2D materials, nonequilibrium Green's functions, quantum transport simulation.

1. Introduction

The discovery of graphene has demonstrated the stability of two-dimensional (2D) materials and paved the way for the fabrication of a plethora of new layered materials with a large variety of properties, as band gap and alignment, effective masses and in-plane anisotropy [MIRÓ 14, ÖZÇ 16, ZHA 17]. The use of 2D materials in nanoelectronics is particularly promising [SCH 15] thanks to the extreme thinness of the layers (down to monoatomic), which allows an optimal electrostatic control, and to the absence of dangling bonds at the surfaces, which reduces the risk of impurities at the interface with the gate oxide and then the presence of detrimental mid-gap states [PALA 13]. The realization of a whole microprocessor based on 2D MoS_2 [WAC 17] is a striking demonstration of the high potentiality of these materials. Additionally, the weak van der Waals (vdW) coupling between the layers allows the fabrication of heterostructures [GEIM 13, LIU 16b, PANT 16], whose properties can be tailored on the basis of those of the constituent materials.

While competition with bulk semiconductors is hard for applications in standard field-effect transistors [FIORI 14, SCH 15], 2D materials may excel in flexible electronics, optoelectronics and low-power electronics [CHO 16]. Here, we focus on this last point and consider the use of monolayer transition metal dichalcogenides for tunnel field-effect transistors (T-FETs) with sub-thermionic subthreshold swing (SS) [JENA 13].

Two alternative architectures of T-FETs based on 2D materials are possible: the planar T-FET and the vertical T-FET. Both of them received much attention in the literature.

Planar T-FETs [ILA 15, ILA 16, LIU 16, AGA 17] are based on a single semiconducting 2D material properly doped to obtain a *p-i-n* junction. The tunneling occurs between the valence band of the source and the conduction band of the channel (or between the valence band of the channel and the conduction band of the drain) through the energy gap between them, whose width is controlled by a gate. Several proposals for this type of device have been made in the literature, most of them with the purpose of improving the transistor performances by a proper tuning of the effective masses and band gaps. In particular, the use of multilayer phosphorene has been suggested in order to achieve, thanks to its intrinsic anisotropy, a small effective mass along the transport direction and a large effective mass

in the transverse direction [CHEN 17b]. This helps increasing the tunneling coefficient and the density of states at the same time, which results in a large ON current. The planar T-FET performances can be also improved by controlled uniaxial strain [SEO 17] or dielectric engineering [ILA 15b].

Experimentally, one of the main difficulties is to fabricate high-quality *p-i-n* junctions, which can be obtained by electrostatic or chemical doping [FAT 16, SUT 14, ROSS 14, CHO 14, XU 15]. Similarly to T-FETs based on bulk semiconductors, 2D material-based T-FETs suffer from a low ON current, which is an intrinsic consequence of the poorly efficient tunneling transmission mechanism and of the fact that tunneling occurs only at the interface between contact and channel (point-tunneling).

The ON current would benefit from a larger tunneling area that is not limited by the transverse section of the device. It is exactly with this objective that 2D material heterostructures were proposed for the realization of vertical vdW T-FETs [LI 14]. The heterostructure 2D materials are selected to obtain a type-II (staggered) band alignment, so that only the valence band (VB) of one layer and the conduction band (CB) of the other are involved in transport. The device switching mechanism is then based on the gate-controlled crossing and uncrossing of the VB and the CB, which allows or impedes tunneling between the two layers. Ideally, tunneling thus occurs over the whole region of overlap between the layers. While very promising [SZA 15, LU 16, CAM 17, DATTA 17], this type of architecture is exposed to many limitations, such as the experimental difficulty of obtaining high-quality interfaces, the mismatch between the lattice constants of the two layers or the rotational misalignment between them. In particular, these last two issues may result in an indirect band gap and then in a reduced tunneling due to lateral momentum mismatch [LU 17, CAO 18].

Experimentally, working vertical T-FETs based on 2D materials have been obtained [SAR 15, ROY 15, NOU 16, ROY 16, LI 17, YAN 17, LIU 17], but the sub-thermionic SS is limited to a restricted bias range, it is far above the predictions for ideal devices and the ON current is rather low. Indeed, as mentioned above, in addition to usual disorder (impurities, grain boundaries, vacancies), heterostructures may suffer from momentum mismatch, which could further degrade their performances.

In this paper, we carry out self-consistent quantum transport simulations to compare the performances of ideal 2D T-FETs with planar and vertical architectures based on two typical semiconducting transition metal dichalcogenides, namely MoS_2 and WTe_2. Figure 1 shows a sketch of the devices together with the corresponding profiles of the top of the valence band (VB) and the bottom of the conduction band (CB) in the ON and OFF states. While in the planar T-FETs tunneling only occurs at the interface between the *p*-doped source and the intrinsic channel (point-tunneling), in the vertical T-FETs it can occur over the whole region where the bands cross (line-tunneling). We do not consider the presence of disorder in order to provide a simple comparison between the basic physical working mechanisms and to illustrate the main differences between the two architectures.
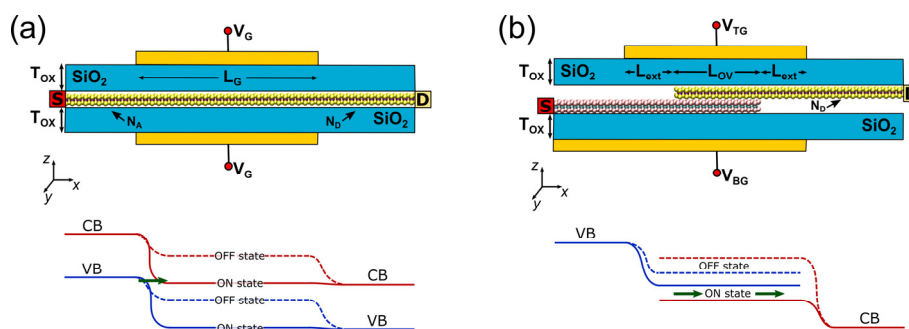
Figure 1. *Sketch of the planar (a) and vertical (b) T-FETs with indication of the main geometrical parameters and illustration of the working principle. The MoS_2 layer is in yellow color and the WTe_2 layer in pink color. The conduction bands are in red, the valence bands in blue. In the simulations, the source (S) and drain (D) contacts are modeled by a periodic prolongation of the layers. The tunneling in the ON state is indicated by arrows in the band profiles.*

2. Description of the devices and simulation approach

We consider MoS_2 and WTe_2 as channel materials for the T-FET. These transition metal dichalcogenides have a convenient band alignment, which makes them appropriate for vertical T-FETs, and have already been considered in the literature [CAO 16, CHEN 17]. The main physical parameters for these materials are reported in Table 1.

	m_c	m_v	E_G	χ
MoS_2	0.467 m_e	-0.633 m_e	1.683 eV	4.30 eV
WTe_2	0.299 m_e	-0.445 m_e	1.092 eV	3.65 eV
MoS_2/WTe_2	0.400 m_e	-0.544 m_e	0.135 eV	

Table 1. *Main parameters (effective mass for the conduction and valence bands, band gap and electron affinity) of isolated and coupled MoS_2 and WTe_2 monolayers. Due to the staggered band alignment, in the MoS_2/WTe_2 heterostructure the WTe_2 VB and the MoS_2 CB form a narrower energy gap. The data for the heterostructure are taken from the DFT calculations of the coupled layers reported in [CAO 16]. We assume the introduction of strain to fit the unit cells of the two materials.*

By using these materials individually or stacked into a vdW heterojunction, we simulate the two alternative architectures of T-FETs reported in Figure 1. Both of them are considered as infinitely extended and invariant along the *y*-direction. The main geometrical parameters are the length of the channel, which corresponds to the intrinsic region under the gate L_G in the planar T-FET and to the overlap region L_{OV} in the vertical T-FET, and the extension length L_{ext} in the vertical T-FET, which corresponds to the lateral lengths of the gate exceeding the overlap region. The doping concentrations are indicated as N_D and N_A for donors and acceptors, and their values will be specified later on. For the planar geometry, we consider a double gate configuration. In the vertical configuration, the top gate controls the switching, while the larger bottom gate electrostatically dopes the bottom (WTe_2) layer and the top (MoS_2) layer is chemically *n*-doped. As gate oxide we consider SiO_2 with thickness T_{OX}=1 nm.

To describe the 2D materials, we make use of *k·p* Hamiltonians for the isolated layers [KOR 15] and of an effective mass Hamiltonian for the coupled layers [CAO 16]. In order to have a fair comparison, we calibrate both models on the density functional theory (DFT) simulations reported in [CAO 16], see Table 1.

Both MoS_2 and WTe_2 show a direct band gap with valleys at the K and K' points of the hexagonal Brillouin zone. The *k·p* Hamiltonian around the K point reads

$$\mathbf{H}(k) = \begin{pmatrix} -\chi - E_G + \alpha k^2 & \gamma(k_x - ik_y) \\ \gamma(k_x + ik_y) & -\chi + \beta k^2 \end{pmatrix} \rightarrow \mathbf{H}(x, k_y) = \begin{pmatrix} -\chi - E_G + U(x) + \alpha k_y^2 - \alpha \partial_x^2 & -i\gamma(\partial_x + k_y) \\ -i\gamma(\partial_x - k_y) & -\chi + U(x) + \beta k_y^2 - \beta \partial_x^2 \end{pmatrix} \quad [1]$$

where $\boldsymbol{k}=(k_x, k_y)$ is the displacement of the wave vector with respect to the K point. As indicated in the equation, we pass to the real space representation by substituting $k_x \rightarrow -i\partial_x$ and keeping k_y as a good quantum number since the system is periodic in the *y*-direction. We also include the electrostatic energy potential $U(x)$ and the electron affinity χ on the diagonal. Note that an equivalent Hamiltonian holds around the K' point, which is the time-reversal conjugated of [1]. Since we do not consider here intervalley scattering, we just make use of Hamiltonian [1] and imply double degeneracy. As for the parameters, we consider γ-values provided by the literature and calibrate E_G, α and β so to reproduce the band gap and effective masses of table 1. We have γ=0.382 eV nm [SEG 16], α= 0.0265 eV nm^2

and $\beta = -0.0051$ eV nm^2 for MoS$_2$, and $\gamma = 0.3$ eV nm [KOR 15], $\alpha = -0.0032$ eV nm^2 and $\beta = 0.0450$ eV nm^2 for WTe$_2$.

When the two materials are stacked into a vdW heterostructure, we just need to consider the VB of WTe$_2$ and the CB of MoS$_2$. Therefore, following [CAO 16] we introduce an effective mass Hamiltonian describing each band and a coupling parameter t between the two

$$\mathbf{H(k)} = \begin{pmatrix} -\dfrac{\hbar^2}{2m_v}k^2 & t \\ t & E_0 + \dfrac{\hbar^2}{2m_c}k^2 \end{pmatrix} \rightarrow \mathbf{H}(x,k_y) = \begin{pmatrix} U(x) - \dfrac{\hbar^2}{2m_v}k_y^2 + \dfrac{\hbar^2}{2m_v}\partial_x^2 & t \\ t & U(x) + E_0 + \dfrac{\hbar^2}{2m_c}k_y^2 - \dfrac{\hbar^2}{2m_c}\partial_x^2 \end{pmatrix} \quad [2]$$

where the coupling parameter t=6 meV [CAO 16] is very small and reflects the weak vdW coupling between the layers, and E_0=134 meV. We assumed that the band gap is direct, i.e. that the valleys of both materials are at the same positions (K and K') in the Brillouin zone. The consequences of indirect band gap are not considered here.

Note that we did not include spin-orbit coupling. Despite its important effects on the band structure, such a crude approximation does not modify our conclusions since the physical mechanisms we simulate are qualitatively not spin-dependent, and both the planar and vertical T-FETs are expected to be affected in the same way by spin-orbit coupling.

In order to perform the simulations, we discretized Hamiltonians [1,2] by finite differences along the x-direction, with a step of 0.1 nm.

The quantum transport simulations are based on the non-equilibrium Green's function approach self-consistently coupled to the Poisson equation for the system electrostatics. The key ingredients of the formalism are the retarded ($\mathbf{G}^R$) and lesser ($\mathbf{G}^<$) Green's functions, which can be obtained, in the channel region, as

$$(E\mathbf{I} - \mathbf{H} - \mathbf{\Sigma}^R)\mathbf{G}^R = \mathbf{I} \qquad \text{and} \qquad \mathbf{G}^< = \mathbf{G}^R \mathbf{\Sigma}^< \mathbf{G}^A \qquad [3]$$

where the retarded ($\mathbf{\Sigma}^R$) and lesser ($\mathbf{\Sigma}^<$) self-energies account for the contacts and the electron-phonon interaction. For the latter, we make use of the self-consistent Born approximation and local electron-phonon coupling, which result in the diagonal self-energies for acoustic and optical phonons

$$\mathbf{\Sigma}_{ap}^<(x,E) = \dfrac{D_{ap}^2 k_B T}{\rho u_s^2} \mathbf{G}^<(x,E) \quad \text{and} \quad \mathbf{\Sigma}_{opt}^<(x,E) = \dfrac{\hbar D_{opt}^2}{2\rho\omega}\Big[\mathbf{G}^<(x,E+\hbar\omega)[n(E+\hbar\omega,T)+1] + \mathbf{G}^<(x,E-\hbar\omega)n(E-\hbar\omega,T)\Big] \quad [4]$$

where ρ is the material density, u_s is the sound velocity, k_B is the Boltzmann constant, T=300 K is the temperature, D_{ac}=3 eV and D_{opt}=2.6x10^8 eV cm^{-1} are the electron-acoustic phonon and electron-optical phonon coupling constants, $\hbar\omega$=50 meV is the energy of the most coupled optical phonon [KAA 12], and n is the Bose-Einstein occupation function, which assumes the phonon bath at thermal equilibrium.

3. Results and discussion

In this section, we compare the results of the simulation of the planar and vertical T-FETs of Fig. 1 with similar geometrical parameters and doping. We set the supply voltage V_{DD} to 0.3 V, as this kind of devices is intended for low-power applications.
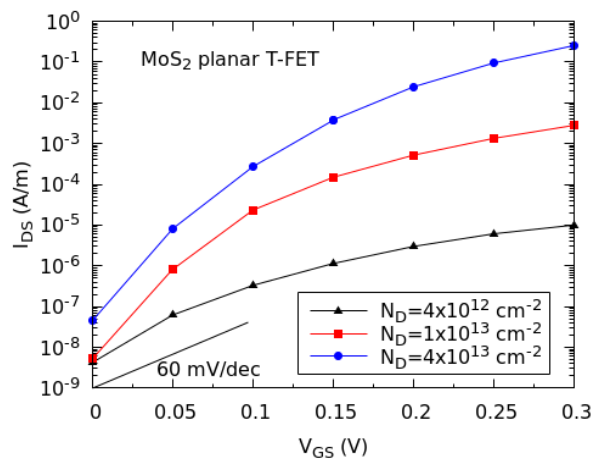
3.1. *Planar T-FET*

In the case of the planar T-FET structure, the main design parameters are the single layer material, the source and drain chemical doping levels N_D, and the gate length L_G. Figure 2 compares the transfer characteristic (source drain current density *per* unit of width I_{DS} as a function of the gate-source potential V_{GS}) of the T-FET based on MoS_2 with that based on WTe_2 for L_G= 20 nm and doping $N_D=N_A=4\times10^{12}$ cm^{-2}. WTe_2 provides a lower SS than MoS_2 and well below the thermionic limit of 60 mV/dec at room temperature. Moreover, it shows an ON current more than 10 times larger than MoS_2. The better performance of the WTe_2-based transistor can be understood in terms of the electronic structure properties reported in Table 1. In particular, the smaller effective masses of both CB and VB of WTe_2 and its smaller band gap allow a larger penetration of electron in the barrier, and consequently a more efficient tunneling. This is particularly beneficial for the ON current, which is strongly limited by the larger MoS_2 gap. Anyway, in both cases and for the design parameters considered here, the ON current is too small for practical applications, despite the decent ON/OFF current ratio larger than 10^4.
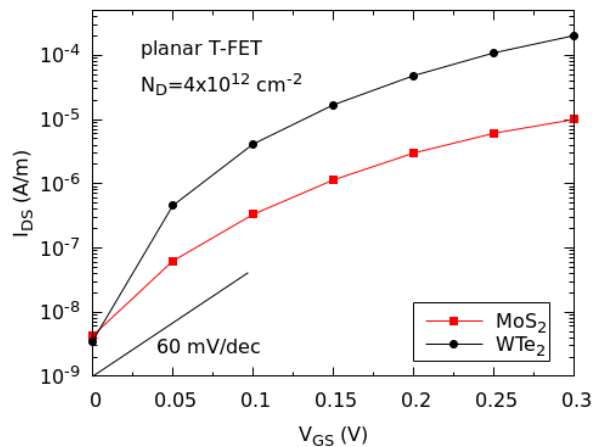

Figure 2. *Transfer characteristics of MoS_2 and WTe_2 planar T-FETs with V_{DD}= 0.3 V, L_G= 20 nm, and the source and drain doping levels $N_D=N_A$= 4×10^{12} cm^{-2}.*

The performances can be improved by increasing the source and drain doping concentration. Figure 3 shows that increasing the doping level up to 4×10^{13} cm^{-2} allows the planar T-FET to provide higher currents. As we can infer from Figs. 4(a,b), which show the local density of states (LDOS) together with the CB and VB profiles in the MoS_2 planar T-FET for two different doping levels and at same gate voltage (V_{GS}= 0.1 V), the origin of this improvement is twofold. From one side, a more degenerate 2D semiconductor entails an upward shift of the source VB with respect to the channel CB, and then opens a larger energy window for tunneling with a larger density of states. From the other side, the higher doping allows a better screening of the gate potential on the source, and the consequent sharper profile of the VB, which decreases more quickly when approaching the channel region, as we can see by comparing the two panels of Fig. 4. As a consequence, the band-to-band-tunneling distance between source and channel is reduced and the tunneling coefficient enhanced. Note that for a higher doping level the increase of the ON current is stronger than that of the OFF current. This leads, for the concentrations considered here, also to a SS improvement.
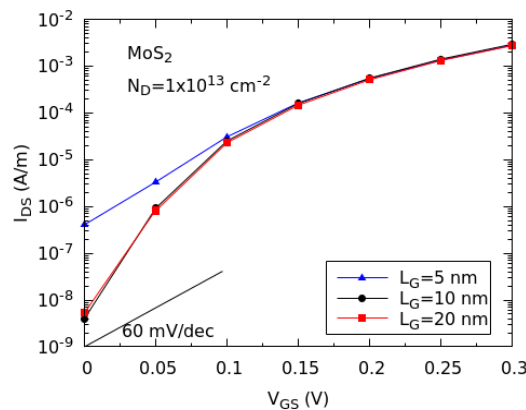
Figure 3. *Transfer characteristics of MoS$_2$ planar T-FETs for different doping levels with V$_{DD}$= 0.3 V and L$_G$= 20 nm.*
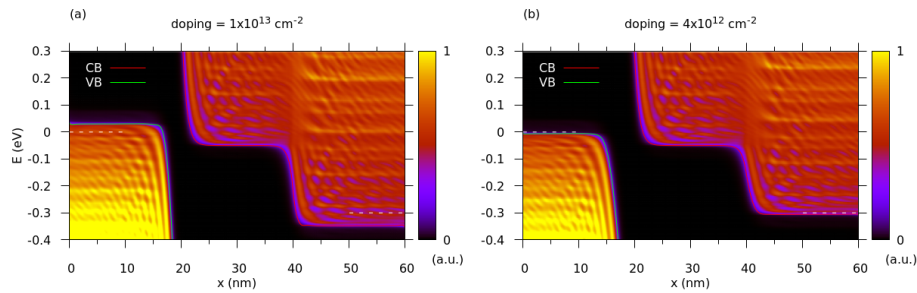
Figure 4. *Local density of states of MoS$_2$ planar T-FETs for (a) N$_D$=N$_A$= 10^{13} cm^{-2} and (b) N$_D$=N$_A$= $4x10^{12}$ cm^{-2} as function of the energy and the longitudinal position. The green and red solid lines indicate the VB and CB, and the left and right white dashed lines indicate the source and drain Fermi levels, respectively.*

We now focus on the dependence of the MoS$_2$ planar T-FET performances on the gate length, which can provide us with information of the possible scalability of these devices. Figure 5 shows the transfer characteristics for L$_G$= 5, 10 and 20 nm. The T-FET appears to scale very well when reducing the gate length from 20 nm to 10 nm, with unchanged performance. Indeed, the electron-phonon coupling does not significantly affect transport through the channel and therefore the current, in both the ON and the OFF states, is almost the same. In the presence of disorder, not considered in our simulations, we might expect a current reduction when increasing the gate length. Importantly, for very short L$_G$ (such as 5 nm in our simulations), the OFF current and consequently the SS degrade significantly, due to the direct source-to-drain tunneling. We conclude that, depending on the specific material (effective masses and band gap), planar T-FETs cannot be too aggressively scaled.
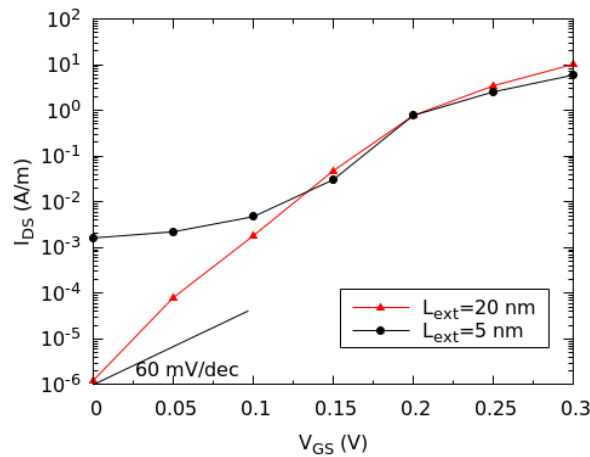

Figure 5. *Transfer characteristics of MoS$_2$ planar T-FETs for different gate length L$_G$ with source and drain doping level of 10^{13} cm^{-2}.*

Our results are in agreement with the results reported in the literature [LIU 17], which are based on atomistic simulations. Note that we did not include spacers (which would separate the source and drain doping region from the gate) in our model. Indeed, the spacers would act as additional barrier regions, thus strongly decreasing the current and deteriorating the device performance due to longer tunneling distance. This effect points to two critical parameters to control in order to optimize the planar T-FET performances, namely the alignment of the gate to the intrinsic channel region, and the sharpness of the *p-i* (or *i-n*) interfaces.
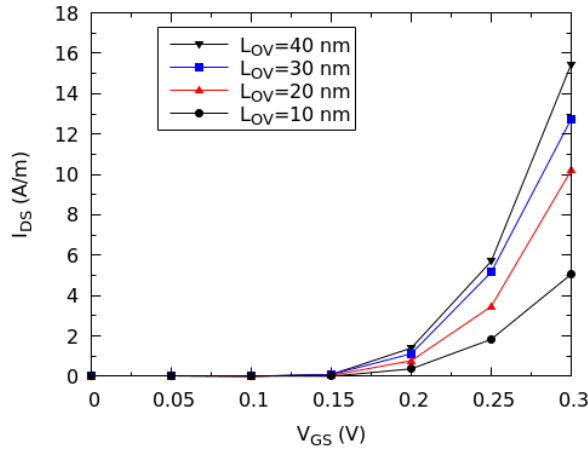
3.2. Vertical T-FET

For the vertical T-FET structure, we consider L_{OV} = 20 nm, N_D= 4x10^{13} cm^{-2} on the MoS$_2$ drain and a back gate potential V_{BG}= -0.5 V, which allows an electrostatic doping of the source WTe$_2$ layer, and is chosen in order to result into a degenerate valence band in the source region [CAO 17]. Among the most important design parameters, we find the length L_{OV} of the overlap region between the two layers, and the gate extension length L_{ext} beyond this overlap region, see Fig. 1. In particular, L_{ext} strongly influences the SS, as shown in in Fig. 6, where we compare the transfer characteristic (I_{DS}-V_{GS}) of vertical T-FET structure with L_{ext}= 5 and 20 nm. While, in the ON regime, the currents are similar in the two cases, the SS and the OFF current are found to be significantly degraded for the shorter extension length, and the device is not able to switch off. As analyzed more in detail in [CAO 16], we can show that, in the OFF state, the CB in the extension region is above the VB within the overlap region. This means that, after tunneling from the bottom WTe$_2$ to the top MoS$_2$ layer, electrons have to tunnel through a gap in the extension region before reaching the drain. Therefore, in the ideal situation considered here (i.e., in the absence of disorder), the current in the OFF state is attenuated exponentially by increasing L_{ext}. On the other side, the interlayer tunneling (in the overlap region) in the OFF state is assisted by the inelastic scattering of electrons with optical phonons [PALA 17], which can promote the electrons to higher energy, thus enhancing electron tunneling from the bottom layer VB to the top layer CB before the crossing of the bands. In what follows, we choose the more performant value L_{ext}= 20 nm.

Figure 6. *Transfer characteristics of MoS$_2$-WTe$_2$ vertical T-FETs for different L_{ext} with V_{DD}= 0.3 V and L_{OV}= 20 nm.*

In the ON state, the inversion of the top layer CB and the bottom layer VB takes place in the whole overlap region. Therefore, the interlayer tunneling occurs over a surface of size L_{OV} times the width of the vertical T-FET. Figure 7 shows the transfer characteristics of vertical T-FETs with different L_{OV}. The ON current is found to scale almost linearly with short L_{OV}. However, for L_{OV} longer than 30 nm, I_{ON} becomes fairly insensitive to L_{OV} and tends to saturate. We speculate that the current flowing along the top layer might be limited by the electrical conductivity of the monolayer material, and not by the overlap length, and in particular by its reduced density of states [SZA 15]. Importantly, such a behavior determines the transition from line-tunneling to point-like tunneling. In such a situation, the only strategy to increase I_{ON} consists in increasing

the device width. Note that for vertical T-FETs whose two layers are very weakly coupled (for example, in the presence of an insulating interlayer barrier, such as an h-BN thin film), I_{ON} is found to scale linearly with L_{OV} over a much larger range of overlap length [CAO 16b]. The reason is that the interlayer tunneling is small, and longer L_{OV} have to be considered before the current is high enough to be limited by other factors. The necessity of a relatively long L_{ext} and L_{OV} limits the scalability of vertical T-FETs. By remarking that only the extension region between the overlap region and the drain plays a role (and so we can set $L_{ext}=0$ for the extension region close to the source), and by considering a minimum overlap length $L_{OV}=10$ nm and $L_{ext}=15$ nm on the basis of Figs. 6 and 7, we estimate that the gate length cannot be shorter than $L_G= 25$ nm for our device to have decent performance.

Figure 7. *Transfer characteristics of MoS$_2$-WTe$_2$ vertical T-FETs for different L_{OV} with V_{DD}= 0.3 V and L_{ext}= 20 nm.*

3.3. Comparison and figures of merit

In this section, we compare the performances of vertical and planar architectures for T-FETs based on 2D materials and with the similar design parameters, namely L_G=20 nm for the planar TFET and $L_{OV}=L_{ext}$=20 nm for the vertical TFET, same source and drain doping level $N_D(=N_A)$=10^{13} cm^{-2}, and V_{DD}= 0.3 V. The I_{DS}-V_{GS} characteristics are shown in Fig. 8. The vertical T-FET outperforms the T-FET by providing a small SS over a larger I_{DS} range, and a larger I_{ON}. Though the band coupling is larger in the planar case, the point-tunneling mechanism strongly limits the current, in contrast to what happens with the interlayer line-tunneling in the vertical T-FET. However, as illustrated above, even in the ideal configuration considered here, the price for a high ON current is the saturation of line-tunneling. On the other hand, an appropriate optimization of the planar T-FET (as the increase doping and the reduction of the gate-oxide thickness) may improve its performance.

In the perspective of circuit realization, we consider two figures of merit to characterize the T-FETs, and in particular the switching energy (E_{SW}) and the delay time (T_{SW}). The former gives information about the energy consumption of the device, and the latter about its velocity [CAO 15]. They are obtained from

$$T_{sw} = \frac{Q_{ON} - Q_{OFF}}{I_{ON}} \qquad \text{and} \qquad E_{sw} = (Q_{ON} - Q_{OFF})V_{DD} \qquad [5]$$

where $I_{ON}=I_{DS}(V_{GS}=V_{DS}=V_{DD})$ by assuming I_{OFF}=10pA/µm, while Q_{ON} and Q_{OFF} are the mobile charges within the channel in the ON and OFF states, respectively.

Figure 9 shows the intrinsic energy-delay figure of the two architectures. The planar structure can provide lower power consumption, while the vertical T-FET allows both low power consumption and a faster switching time. Note that the short delay time of the vertical T-FET is obtained thanks to the high ON current and despite the charge is larger than for the planar T-FET. For reference, in Fig. 9, we also compare these two structures to high-performance (HP) CMOS. The vertical T-FET turns out to be better in terms of both power and speed.

Our analysis refers to the ideal case and does not take into account the role of parasitic capacitances and of the presence of interconnects.
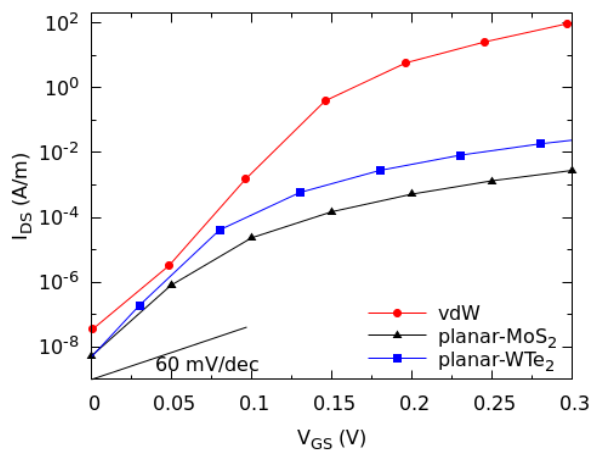
Figure 8. *Transfer characteristics comparing the MoS$_2$-WTe$_2$ vertical vdW T-FET with the MoS$_2$ and WTe$_2$ planar T-FETs with source and drain doping level of 10^{13} cm^{-2}, L$_G$=20 nm for the planar T-FET and L$_{OV}$=L$_{ext}$=20 nm for the vertical T-FET.*
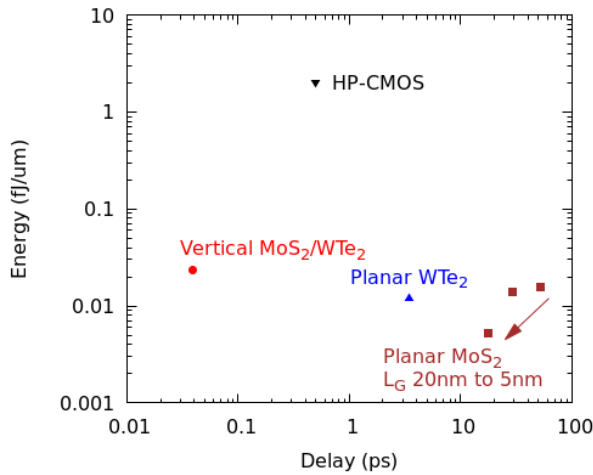
Figure 9. *The energy delay of planar MoS$_2$ and WTe$_2$ T-FET and MoS$_2$-WTe$_2$ vertical T-FET.*

4. Conclusion

By means of self-consistent quantum transport simulations based on effective mass and *k·p* models, we compared the physics and the ideal performances of the alternative planar and the vertical architectures for T-FETs based on 2D materials. From the device point of view, the main difference between the two geometries is that the band coupling is larger in the planar one, but transport occurs through point-tunnelling, which limits the current compared to the line-tunnelling observed in planar T-FETs. This results, at least for the parameters considered in our simulations, in a better performance of vertical T-FETs and in particular in a higher ON current. For their part, planar T-FETs are expected to offer better scaling possibilities. The presence of disorder, not considered here, might affect our results, which are however indicative of the basic differences between the two architectures and could serve as a first guide for the transistor design. While more performant, vertical T-FETs might be more sensitive to disorder, thus requiring the experimentally challenging realization of clean van der Waals heterostructures.

Acknowledgements

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