SiGe based line tunneling field-effect transistors

Experimental properties and characteristics

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ABSTRACT. In this paper we report on our progress with SiGe gate-normal / line tunneling FETs, highlighting recent advancements by the example of three transistor concepts. We demonstrate the unique characteristics shared by these transistors, such as the on-current proportionality to the source-gate-channel overlap area and explain the obstacles imposed by fringing fields leading to parasitic tunneling at the edges of the tunneling area. Our experimental results show that adding counter doping to the channel provides an efficient means to mitigate penalties to the subthreshold swing caused by parasitic tunneling paths and additionally helps to improve the on-current and I_{on}/I_{off}-ratio. Moreover, we point out the dependence of the superlinear onset on the tunneling transmission probability with a focus on the doping profile at the tunneling junction. We consider the role of traps on the subthreshold swing within the scope of temperature dependent electrical measurements. Furthermore, we show that by avoiding ion implantation and hence crystal defects as much as possible, smaller minimum subthreshold swings can be reached. At last, taking the experience acquired on the three transistors concepts into consideration, we propose an advanced TFET concept.
KEYWORDS. TFET, line tunneling, trap assisted tunneling, superlinear onset, counter doping.

1. Introduction

Tunneling field-effect transistors (TFETs) bear the fundamental capability of achieving sub-60 mV/dec switching at room temperature, the physical limit inherent to the MOSFET operation principle. By exploiting these steep slope characteristics, a significant power reduction based on supply voltage (V_{DD}) scaling is anticipated for a potential use of TFETs in future integrated circuits (IC). Accordingly, a diverse field of TFET research has developed, including studies on Group IV materials [CHOI 07, KNO 13], III-V semiconductors and heterojunction designs [TAK 16, MEM 16b], nanowires [MEM 16a], 2D materials [JENA 13, SAR 15], gate-oxide scaling [AHN 17], pocket doping [BLA 15], electron-hole bilayer FET [LAT 12] and alternate architectures. Concerning TFET architecture, the so called gate-normal or line tunneling concepts have attracted attention, due to their potential to achieve higher on-currents and better average SS than conventional designs [AGA 10]. In these transistors the tunneling path is aligned with the electric field of the gate. The design is a means to increase the extent of the tunneling junction taking on the challenge of low on-currents, caused by small tunneling probabilities in indirect semiconductors.

The idea of gate-normal tunneling was first mentioned in refs. [BOW 08, PAT 09] in the framework of simulations analyzing a configuration where the source doping region undercuts the gate with an ultra-shallow pocket of opposite dopants sandwiched between gate and source. Much work was initially performed on the III/V-system, where line tunneling FETs (L-TFETs) were demonstrated using InP/InGaAs [ZHOU 11], as well as AlGaSb/InAs achieving on-currents close to 80 µA/µm [LU 12] and even exceeding 180 µA/µm [ZHOU 12] in InAs/GaSb TFETs. Moreover, distinct TFET characteristics like NDR were shown in experiment [YU 13]. A multitude of simulations was performed, e.g. concerning the optimal geometry and electrostatics of III/V L-TFETs [LI 12, HSU 16]. Detailed theoretical studies investigating the turn-on abruptness of L-TFETs in dependence of source doping, pocket doping, oxide thickness, gate alignment and materials taking quantum confinement into account were contributed in

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refs. [KAO 12, KAO 13]. From the same institution, experimental work on SiGe/Si was published [WAL 14] and the performance of L-TFETs in small circuits such as current mirrors was considered recently [MAR 17]. In addition, detailed analysis on Si, SiGe and Ge heterostructures, on band offsets therein and on controlling tunneling paths were performed theoretically in detail by Hsu *et al.* [HSU 13, HSU 15]. The work presented in this paper focuses on recent experimental results acquired with SiGe L-TFETs [SCHM 14, BLA 15, GLA 17b].

2. Concept of line tunneling FETs

Figure 1 shows a comparison of a point tunneling [Figure 1 (a)] against a line tunneling [Figure 1 (b)] FET by TCAD simulations, where both devices have the same dimensions, equal doping concentrations and equal outer electrical parameters are applied ($V_g = 0.5\,V, V_D = 0.25\,V$). The important difference lies in the direction and position of the tunneling junction. In Figure 1(a) the tunneling junction lies perpendicular to the gate at the interface between p-Si source and i-Si channel. In Figure 1(b) the source undercuts gate and channel and thus forms an interface parallel to the gate, such that the tunneling path is normal to the gate. Since the generation of tunneling carriers in Figure 1(a) is constrained to a small circular area, decaying rapidly from the point of maximum electric field, devices with such geometry are referred to as point tunneling devices. In the case shown below ($EOT = 0.8$ nm, $WF = 4.2$ eV) the tunneling rate decreases on the order of 10^3 if the distance from the tunneling junction is increased by 2 nm. Likewise, the term line tunneling FET is used for devices where a 2D line of parallel tunneling paths with similar tunneling probabilities can be found as shown in Figure 1(b). Since the magnitude of the electric field in the channel decreases immensely perpendicular to the gate, it is crucial to keep the channel thickness in the range of 5 nm or less in order to gain maximum tunneling rates. The idea behind line tunneling FETs is to increase the junction area and hence the drive-current of the transistor while keeping its overall dimensions constant, as shown in Figure 1.

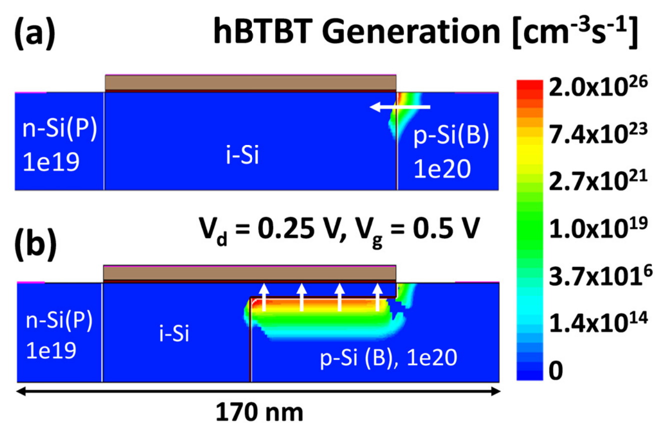

Figure 1. *Hole band-to-band tunneling generation rate in a point tunneling based device (a) and a line tunneling based device (b). In (a) the tunneling rate peaks at a single point, where i-Si channel, p-Si Source and HfO_2 gate touch. In (b)* 3 nm *below the gate and parallel to the interface with the channel, a 2D-line of equal tunneling probability is found.*

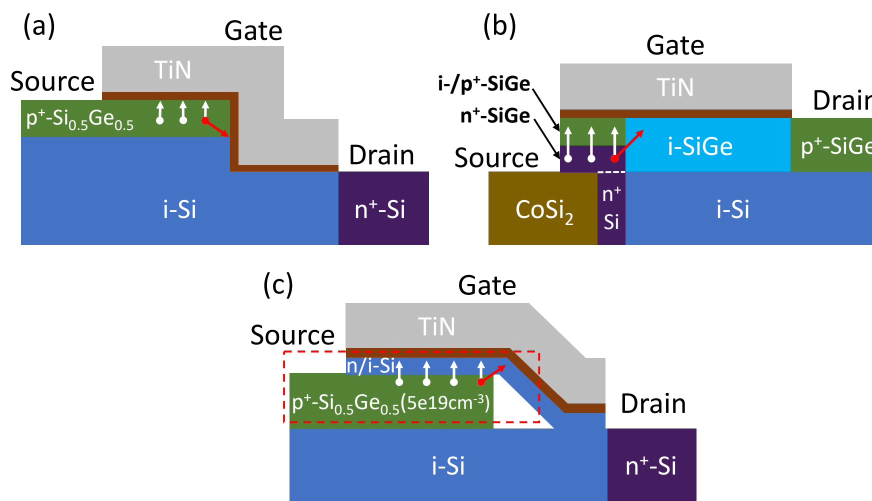

Figure 2. *Three different concepts to achieve line tunneling, (a) by inverting a moderately doped source (n-TFET)* [SCHM 14], *(b) at an n^+p^+-SiGe junction (p-TFET)* [BLA 16] *and (c) in a heterojunction n-TFET* [GLA 17b]. *In each figure the line tunneling paths are delineated by white arrows and a parasitic tunneling path caused by elevated fringing fields at the edge of the line tunneling area is indicated in red.*

3. Line Tunneling FET designs

Realizations of L-TFETs may rely on different tunneling junction concepts as shown in Figure 2. The junction in Figure 2(a) is created by inversion of the SiGe source in close proximity to the SiGe/gate dielectric (HfO_2) interface. This imposes a limit to the maximum value of the doping concentration [SCHM 14]. In case of excessively large doping ($> 5 \cdot 10^{19}\ cm^{-3}$), inverting the source electrostatically through the gate is inefficient, resulting in a small I_{on}/I_{off}-ratio. On the other hand, high source doping is needed to achieve a high tunneling probability and on-current, which makes it a challenge to meet all the requirements for high efficiency. The tunneling junction of the L-TFET displayed in Figure 2(b) is composed of an n^+p^+-junction within a $Si_{0.45}Ge_{0.55}$ layer [BLA 15, BLA 16], whereas in the device shown in Figure 2(c) a $Si_{0.5}Ge_{0.5}$/Si hetero interface is present at the tunneling junction [GLA 17b]. The line tunneling paths are schematically indicated by white arrows in each figure, all pointing in the direction perpendicular to the gate. In each concept a potential parasitic tunneling path is emphasized by a red arrow, indicating a direction of elevated electric fields (fringing fields) at the edge of the tunneling layer.

4. Results and Discussion

In the following paragraphs conclusions are drawn on the particularities of switching in L-TFETs. The findings of the next section are general and applicable to all transistors shown in Figure 2, but exemplary derived from the structure shown in Figure 2(c). In the subsequent sections we also derive inferences by comparison of the different tunneling junction designs, regarding source and channel doping, as well as crystal defects leading to trap states.

4.1. *Characteristics of L-TFETs*

The significant tunneling paths that contribute to the device current in L-TFETs can be illustrated with the help of simulated transfer characteristics and two electron band-to-band tunneling generation (eBTBT) plots taken at distinct V_g as displayed in Figure 3. The plots were acquired from 2D Sentaurus TCAD simulations using a non-local BTBT model, where details can be found in [TCAD 14, GLA 17a]. In the transfer characteristics in Figure 3(a) for three different gate-source-channel overlap lengths d_{gs} (50 nm, 250 nm, 1250 nm) a good agreement between all curves is observed in the early subthreshold

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regime, while a split occurs for $V_g > 0.35$ V. It is expected from theory that by the use of line tunneling the on-current $I_{on} \propto d_{gs}$ and thus an increase of d_{gs} by a factor of five leads to increase of I_{on} by the same amount, as seen in the range between 0.8 V to 1.0 V in Figure 3 (a). In turn, this means that only I_{on} is governed by line tunneling, since the dependence weakens below 0.8 V and is completely absent below 0.35 V, were the curves overlap proofing the independence of d_{gs}. Figure 3(b) emphasizes that at 0.2 V only a tunneling path at the corner of the source region has developed, which is identical for all values of d_{gs}. At this corner the electric field $\vec{E}$ fringes leading to elevated field values, thus stronger band bending and ultimately a premature formation of a tunneling window in comparison with the line tunneling junction. Such a parasitic tunneling path naturally occurs in all designs and is indicated in by a red arrow in each panel of Figure 2. It is a matter of doping, electrostatic design or even work function adjustment to suppress this tunneling path or shift its onset closer to the line tunneling onset [KAO 12, HSU 16]. In order to avoid a degraded average SS, by a kink in the transfer characteristics the onsets of both tunneling paths need careful consideration. At around 0.35 V in Figure 3(a) (marked by a red circle) line tunneling starts to kick with contributions from along the complete line of the gate-source-channel overlap region. In the eBTBT-plot shown in Figure 3(c) the line tunneling paths are fully developed and contribute predominantly to the current of the device. In this example, for the purpose of easy distinction the simulation parameters are chosen such that the two tunneling contributions are well separated in the transfer characteristics. For the sake of performance, especially considering average SS the opposite needs to be aimed at in experiment, which is part of the discussion in the next paragraph.

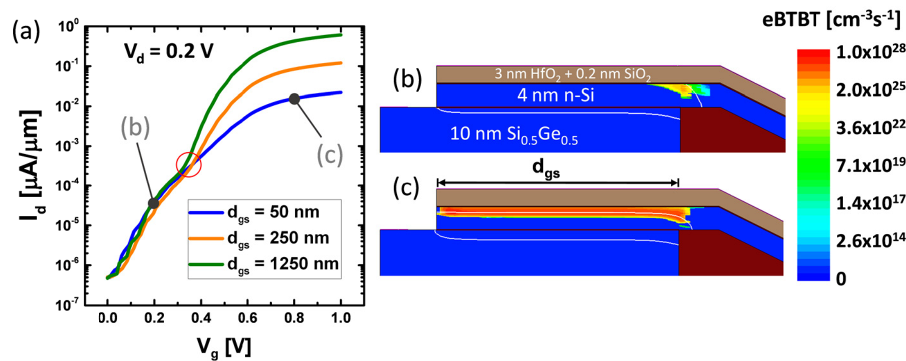

Figure 3. *(a) Simulated transfer characteristics with two distinct points marked, at which the electron band-to-band tunneling generation rate is displayed (b,c) in a close-up of the tunneling junction of Figure 2(c) (red rectangle). At $V_g = 0.8\ V$ a high line tunneling BTBT generation has developed at the gate interface, while in the current in the early subthreshold regime at $V_g = 0.2\ V$ stems from a parasitic tunneling path that develops due to the high electric field at the corner of the source layer. For simulation we assumed an $EOT = 0.8\ nm$ and a channel thickness $t_{channel} = 4\ nm$.*

4.2. *Transfer characteristics*

Figure 4(a) shows experimentally acquired transfer characteristics on TFETs as shown in Figure 2(c), exhibiting many of the properties elucidated in the previous paragraph. The solid lines correspond to TFETs produced on the same chip, but with different gate-source-channel overlap area A_{gs}, with the orange and blue curves corresponding to $A_{gs} = 59\ \mu m^2$ and $A_{gs} = 127\ \mu m^2$, respectively. Similar to Figure 3(a) the curves well match in the subthreshold regime and split in the on-state of the transistor where the total current is dominated by line tunneling. In the inset a magnification of the same curves normalized to A_{gs} between $V_g = 0.75\ V$ and $V_g = 1.5\ V$ provides proof for the scaling of I_{on} with A_{gs} as reported in simulations. Furthermore, the curves for transistors with intrinsic channel (green symbols) in Figure 4(a) illustrate the huge penalty of mismatched tunneling onsets. Compared to

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devices with the same dimensions, but n-doped channel [Figure 2(c)] (orange lines) much worse figures of merit are obtained. In terms of numbers the counter doped devices achieve average SS over four decades of I_d down to $87\,mV/dec$, while devices with intrinsic channel do not go below $245\,mV/dec$. The mean improvement of SS_{ave} between the two species amounts to a factor of 2.4. Additionally, I_{on} is a factor of 2.5 higher and the I_{on}/I_{off}-ratio is improved by more than one order of magnitude. The improvement in SS shows a correlation between the onset voltage and average SS as shown in Figure 4(b). This correlation suggests that the average SS of devices with intrinsic channel is worse, because parasitic tunneling paths set in at much lower V_g than line tunneling. As stated in the previous section, it is of importance to control the onset of parasitic tunneling paths, in this case a diagonal tunneling path as shown in Figure 2(c), 3(b). In simulations an onset mismatch leading to large average SS as for the devices with intrinsic channel (green symbols) can be triggered by even smallest geometric non-idealities on the order of a few nm at the boundary of the source tunneling layer [GLA 17a]. These geometric variations and potentially other non-idealities such as traps cause enhanced electric fields resulting in stronger band bending in a direction diagonal to the gate, along which, a tunneling path develops prematurely. This effect is found to be much more severe for un-doped channels. For counter doped channels, the initial band banding caused by the dopant atoms is much stronger and thus a weaker impact on the band bending is observed making the junction less susceptible to the non-idealities faced in experiment.

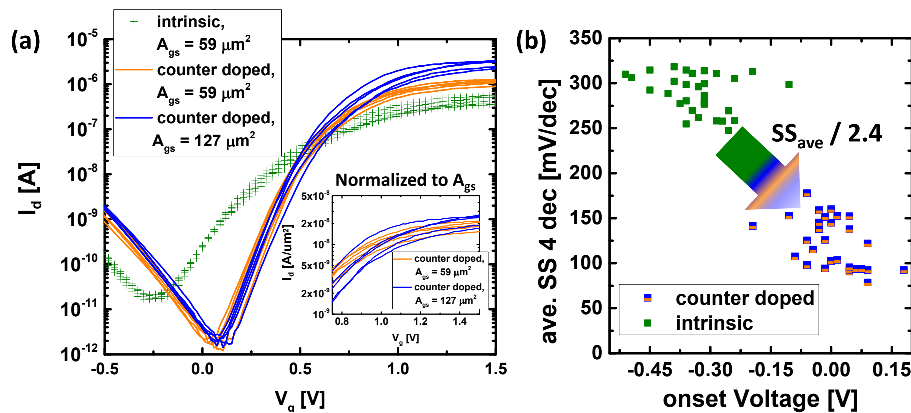

Figure 4. *(a) Comparison of the five best performing devices of three groups of TFETs with counter doping (solid lines) and without counter doping (symbols). Upon increasing the source-gate-channel overlap area A_{gs} from $59\ \mu m^2$ (orange) to $127\ \mu m^2$ (blue) an increase in on-current is observed. The inset shows that I_{on} scales with A_{gs}. A shift in onset voltage and significant improve in SS_{ave} results from counter doping, as quantified in (b). The mean value of $SS_{ave}^{4\,dec.}$ improves by a factor of 2.4.*

4.3. *Output characteristics*

Many TFETs show a superlinear onset in the output characteristics like the ones shown in Figure 5(a) for a device as displayed in Figure 2(a). The superlinear onset may be rooted in a modulation of the tunneling probability with V_d or a change in the occupancy of the allowed density of states in the source region. As described in ref. [MIC 12] the latter occurs when the quasi Fermi energy in the source $E_{F,s}$ at high V_g and $V_d = 0$ is too close to the band edge. In this case most allowed states in the source / valence band [Figure 2(a)/5(a)] are occupied. When V_d increases, $E_{F,s}$ and the band occupancy can be altered, and hence more initial states are available for a tunneling event. This may cause an exponential increase of the tunneling current at small values in a V_d-sweep. For many applications in analogue and digital circuits a linear relation of I_d on V_d is inevitable in order to apply the known rules to the circuit design. Consequently, a linear onset needs to be achieved, which is well possible as evidenced by the output characteristics in Figure 5(b) on a device corresponding to Figure 2(b). Here the source is degenerate and fulfills the condition $CB_{s,min} < E_{F,s} - 3k_BT$, where $CB_{s,min}$ is the conduction band

maximum in the n+-SiGe source [see Figure 2(b)] and $k_B T$ the thermal energy. Thus, there is a sufficient amount of initial tunneling states available at $V_d = 0$ and the tunneling current depends linearly on the voltage drop between source and drain. Furthermore, the optimized source doping in addition to the use of counter doping at the tunneling junction results in an improved on-current. Around 10 $\mu A/\mu m$ can be reached at V_{dd} = -0.5 V. Similar to the results from the previous section the best performance is obtained by the use of counter doping in the channel [Figure 2(b)], based on a stronger band bending and improved resilience against fringing fields.

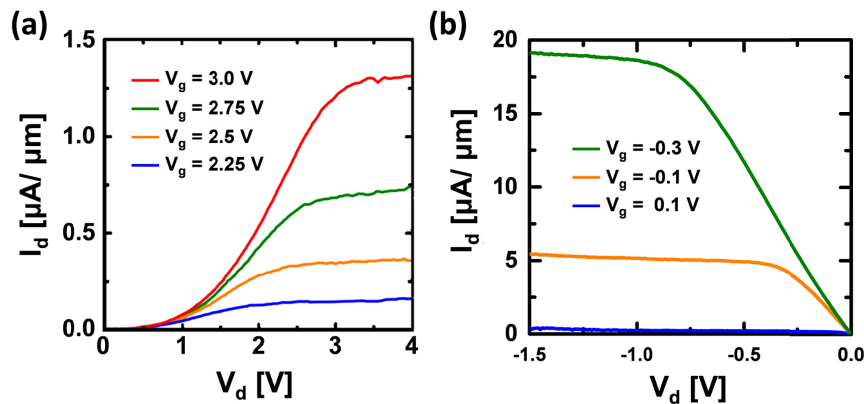

Figure 5. *Output characteristics corresponding to Figure 2(a,b). In (a) a characteristic superlinear onset is observed due to the low source doping, which is necessary for the ability to deplete the source electrostatically. Resulting from the low doping the occupancy function of the source and tunneling length are modulated with V_d. The superlinear onset is suppressed in (b) by higher source doping and a highly transparent tunneling junction formed with the help of counter doping.*

4.4. *Temperature analysis and trap-assisted tunneling*

The presence of trap states in proximity to the tunneling junction has been identified as a heavy source of SS degradation through the mechanism of trap-assisted tunneling (TAT) in many works [VANDO 14, SANT 16]. Hence, much attention has been and continues to be devoted to analyzing and identifying trap states to consequently avoid TAT. With the help of temperature dependent electrical measurements, the dominant physical mechanisms contributing to the current in TFETs at different V_g can be distinguished as shown in Figure 6. In Figure 6(a) transfer characteristics at 100 K, 200 K, 300 K and 400 K are displayed for $V_d = -0.1\,\text{V}, -0.5\,\text{V}$. Assuming an exponential Arrhenius-dependence of the current $I = I_0 e^{-E_a/k_B T}$ on $k_B T$, where I_0 is the current through the device at 0 K, thermal activation energies E_a have been extracted from the temperature dependent measurements and plotted as a function of V_g in Figure 6(b). In the range between $-1.5\,V < V_g < -0.25\,V$ only a slight change in the on-current is observed [Figure 6(a)] as a function of temperature, which corresponds to a low E_a in Figure 6(b) and indicates a predominance of BTBT in this region. For $-0.25\,V < V_g < 0.25\,V$ the SS decreases with temperature, though never crosses the thermal line $k_B T/q \cdot \ln(10)$. Nevertheless, the improvement of SS down to 30 mV/dec shows that the device is not inherently limited from a material and structural point of view, but rather by TAT as seen in Figure 6(b). TAT is associated with an energy range of $0.1\,eV < E_a < 0.35\,eV$ and is dominant in the subthreshold regime around $V_g = -0.2\,V$. Still, it is striking that only a few data points are located in the TAT region and the transition from BTBT to the off-state where Shockley-Read-Hall (SRH) generation of carriers starts to become relevant, is very sudden. An infinitely sharp transition from the off-state to BTBT is the ideal case for a TFET. Hence, the sharp transition observed here, is the key point reflecting the cause for a good average slope of 80 mV/dec over four orders of I_d. Eventually further reduction of traps is needed to reach $< 60\,mV/dec$ switching.

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In this sense we see an improvement in minimum SS (SS_{min}) for our L-TFETs by avoiding crystal damage and thus bulk traps. Table 1 displays SS_{min} for all three transistors seen in Figure 2. Due to the direct implantation of dopants into the source at the tunneling junction of the device in Figure 2(a), severe crystal damage is caused, which cannot be fully recovered by annealing, leaving a significant number of defects and thus parasitic energy states in the bandgap. Therefore, SS_{min} amounts to $150\ mV/dec$, which is double the value achieved for devices corresponding to Figure 2(b) ($75\ mV/dec$). As seen in the evaluation of the temperature dependent measurements the latter devices do not suffer from TAT severely, allowing for smaller SS_{min}. In these devices the source doping is not applied by direct implantation, but rather by implantation into silicide with a subsequent dopant drive out. Thereby, defects at the junction can be reduced. Below $60\ mV/dec$ switching was observed in TFETs where the tunneling junction doping profile was created in-situ during growth [Figure 2(c)]. Here, the least number of traps is expected which becomes noticeable in SS_{min} down to $55\ mV/dec$.

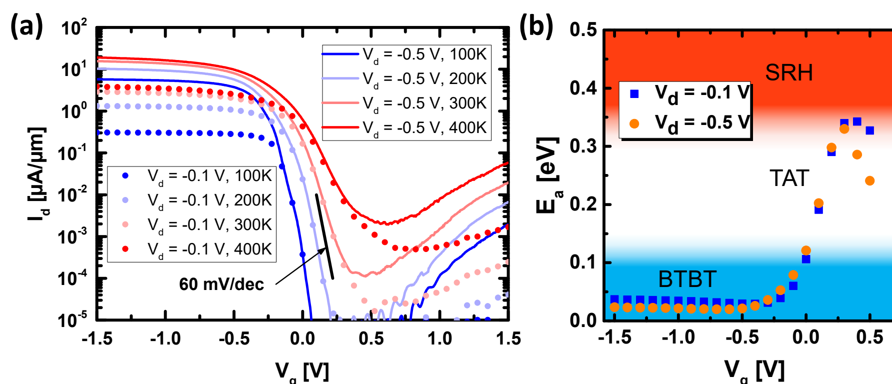

Figure 6. *(a) Temperature dependent transfer characteristics of an LTFET structure as shown in Figure 2(b). TAT limits the subthreshold swing, but is an issue only in a small V_g-range as seen in (b). The sharp transition seen here, is the reason for the excellent average SS of 80 mV/dec over 4 orders of I_d at room temperature.*

Doping method	Implantation [Figure 2(a)]	Implantation into Silicide [Figure 2(b)]	In-situ [Figure 2(c)]
SS_{min}	**150 mV/dec**	**75 mV/dec**	**55 mV/dec**

Table 1. *Minimum SS achieved for tunneling junctions formed by different methods (see Figure 2), especially regarding junction doping. Smaller SS_{min} is observed when trap states are avoided at the tunneling junction, achieved by substituting direct ion implantation by implantation into silicide (150 mV/dec → 75 mV/dec) and by avoiding ion implantation completely, using in-situ doping instead (75 mV/dec → 55 mV/dec).*

5. Outlook

Taking the experience from the previous L-TFETs into account a new structure was proposed of which a sketch is displayed in Figure 7. The doping of all layers in the stack is incorporated during growth to avoid TAT caused by crystal defects created during ion implantation. A high source doping of $2 \cdot 10^{20}\ cm^{-3}$ is employed to achieve a linear onset in the output characteristics. The tunneling junction uses a SiGe/Si heterostructure and is fabricated in two different variants, with and without counter doping to different levels. The concept itself is not limited to the materials shown below, so that the use of lower bandgap materials such GeSn and Ge are feasible.

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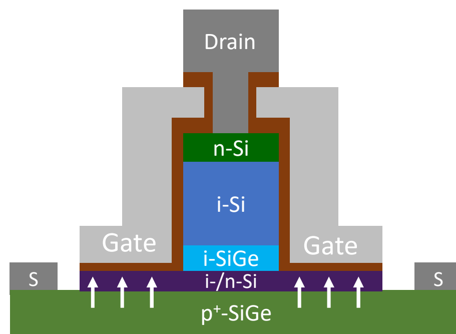

Figure 7. *Proposed L-TFET design for further experimental investigations. The structure incorporates all the elements that were found beneficial in our preceding experiments, such as in-situ doping, counter doping, high source doping and SiGe/Si hetero tunneling junction.*

6. Conclusions

A series of studies on line tunneling FETs was presented and discussed. The common features found for all designs are the on-current scaling properties with the gate-source-channel overlap area and the occurrence of parasitic tunneling paths at the boundary of the source tunneling layer. The latter issue was successfully circumvented by merging the onset of parasitic and line tunneling paths, in addition to a reduction of the susceptibility to fringing fields at the source edges, through the use of counter doping. As a result, $SS = 87\, mV/dec$ for n-TFETs and $SS = 80\, mV/dec$ for p-TFETs averaged over four orders of magnitude of I_d were achieved. Moreover, counter doping enhances the tunneling probability making on-currents on the order of $10\, \mu A/\mu m$ accessible. From the analysis of thermal activation energies BTBT was shown to dominate the on-state of the TFET, while TAT only plays a role in a small range of the subthreshold regime. A clear improvement of SS_{min} was observed through preventing TAT by moving from direct implantation into the source, to using implantation into silicide and ultimately to in-situ doping, where subthermal switching was observed. Moreover, we elucidated the suppression of the superlinear onset in the output characteristics of TFETs by choosing a sufficiently high source doping. As a result of these experiments a TFET design combining the beneficial elements of the investigated devices with high flexibility was proposed and described.

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