The impact of the temperature on In0.53Ga0.47As nTFETs

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ABSTRACT. In this paper, a comparative study between the use of spin on glass and gas phase Zn diffusion of the p++ source of InGaAs TFETs was performed. The use of Zn gas phase doping at the source reduces the tunneling length which results in an enhancement of ION, higher transistor efficiency and intrinsic voltage gain at lower voltages.

The main parameters of gas-phased-diffused In0.53Ga0.47As nTFETs with gate stacks composed by 3 nm or 2 nm HfO2 on top of 1 nm Al2O3 have been analyzed. The resulting equivalent oxide thickness (EOT) was about 0.8 nm and 1.0 nm, respectively. The lower EOT improves the electrostatic coupling, resulting in a lower SS (sub 60 mV/dec at room temperature) leading to a higher gm/IDS in weak conduction. TCAD simulations have shown that the ambipolar effect is significant for higher VDS, degrading SS and consequently gm/IDS in the weak conduction regime, also shifting the gm/IDS peak to higher VGS direction due to the increase of IOFF. The AV peak is strongly degraded by an increase of the temperature due to the increase of the trap-assisted-tunneling (TAT) and Shockley-Read-Hall (SRH) generation mechanisms. For higher VGS the AV is lower, and at the same time less sensitive to temperature variations, which is a favorable regime for temperature-dependent analog operation.

KEYWORDS. TFET, Temperature, Analog parameters, Current conduction mechanisms, intrinsic voltage gain, sub-60mV/dec.

Introduction

Tunnel field effect transistors (TFETs) are devices with Band-to-Band Tunneling (BTBT) as the main current conduction mechanism and their structure consists of a gated p-i-n diode [1]. The advantage of the BTBT mechanism is the capability to reduce the subthreshold swing (SS) to values lower than 60 mV/dec [2-4], the theoretical thermal limit of conventional MOSFETs at room temperature and providing also lower power consumption. Sub 60 mV/dec TFETs have already been demonstrated experimentally as reviewed in [5].

Even with promising switching speed and low power consumption observed, the on state current (I_{ON}) of Si TFETs is not meeting the required target specifications due to the high Si bandgap (1.12 eV). Different source and channel material, such as Ge-based compounds [6-9] and III-V alloys [10-14], offering a lower bandgap than Si, can be used in order to improve I_{ON}. The vertical $In_{0.53}Ga_{0.47}As$ device approach proposed in [10] uses the same material layer structure as the horizontal devices studied in this work.

Electronic devices used in military, aerospace and other applications may need to endure greater environmental variability, including temperature range. The study of the temperature dependence of the device characteristics is important because it allows to evaluate the suitability of their use in harsh operation conditions.

Generally TFETs are more sensitive to defects than MOSFETs, since the off state current (I_{OFF}) is very dependent on trap-assisted-tunneling (TAT) and Shockley-Read-Hall generation (SRH). BTBT generation has only a small relative temperature (T) influence, mainly caused by temperature-dependent bandgap narrowing. However, SRH and TAT generation are thermally activated, increasing

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exponentially with the temperature. Conversely, characterization at different temperatures enables to identify which of the conduction mechanisms is dominant [15, 16].

Although TFETs are excellent alternatives for logic applications due to their improved switching characteristics and lower power consumption, TFETs have already shown to be promising in analog applications [17-25]. Comparisons between TFETs and MOSFETs in [22,24] have shown better analog performance of TFETs, and some basic circuits using TFETs have already been studied [26-29] highlighting their promising characteristics.

In this work, initially, a comparative study between two Zn diffusion processes (solid-source and gas-phase diffusions) for the source doping of InGaAs TFETs is done. Then, the influence of the temperature on the main parameters of InGaAs TFETs with the Zn diffusion made with Gas Phase is studied, for 2 different HfO_2 thicknesses (3 and 2 nm).

Device Characteristics

In this work n-type $In_{0.53}Ga_{0.47}As$ homo-junction TFETs are analyzed, where the source doping is made by spin-on-glass (solid-source diffusion) or by Zn gas-phase diffusion. These devices are inspired on the original approach from the University of Tokyo [11,30], optimized by Alian et al. in [31] using solid-source diffusion, and in [32] using gas phase diffusion. A schematic representation of the $In_{0.53}Ga_{0.47}As$ devices is presented in figure 1.

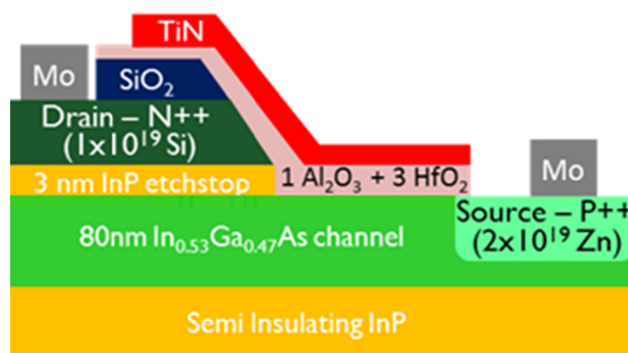

Figure 1. *Representation of the $In_{0.53}Ga_{0.47}As$ nTFET used.*

Two different splits with gate stacks composed by 3 nm or 2 nm of HfO_2 on top of 1 nm Al_2O_3, with TiN as the metal gate were analyzed. The equivalent oxide thickness of the 2 nm HfO_2 is about 0.8 nm and of the 3 nm HfO_2 device is about 1.0 nm. The P++ source is doped with Zn, using gas phase or spin-on glass diffusion. Both diffusions were made at 500ºC for 1 minute. The drain is doped with Si (N++). More details about the process can be found in [31,32].

Analysis and Discussion

Figure 2 presents the experimental normalized drain current (I_{DS}/W) as a function of gate voltage (V_{GS}) for the $In_{0.53}Ga_{0.47}As$ with the Zn source diffusion made by spin on glass and by gas phase, for two different drain voltages (V_{DS}). It is possible to observe that the gas phase device present higher I_{ON}. This higher I_{ON} is related to its higher source/channel junction abruptness that is a result of the different Zn diffusion processes, causing a reduction of the tunneling length.

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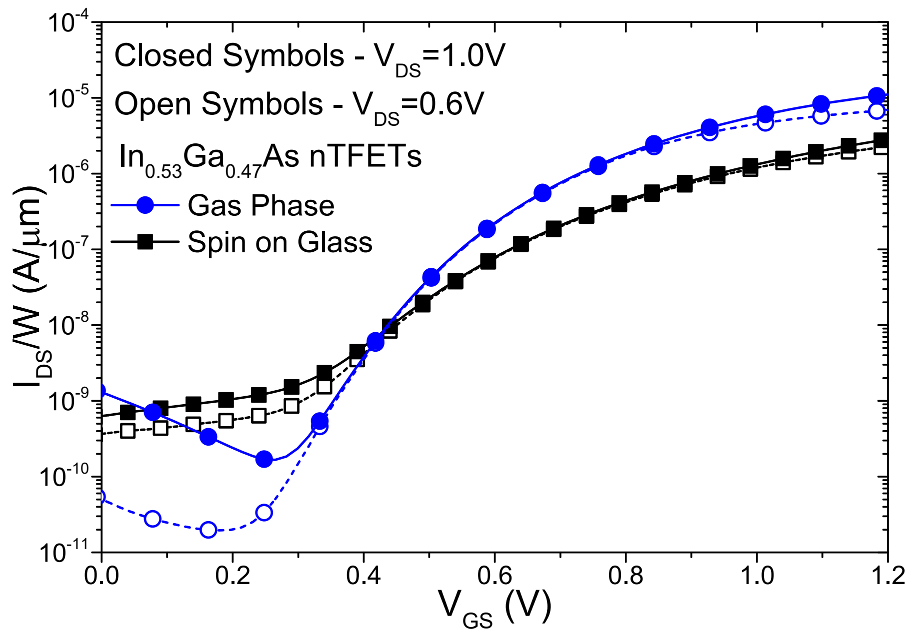

Figure 2. *Experimental normalized I_{DS} as a function of V_{GS} for $In_{0.53}Ga_{0.47}As$ nTFETs, with different Zn diffusion processes of the source.*

One important figure of merit is the transistor efficiency (gm/I_{DS}), where it is possible to observe the analog characteristics of the transistor in different operation regimes. Figure 3 present gm/I_{DS} as a function of the normalized I_{DS} for both Zn diffusion processes at the source. The gas phase device presents higher gm/I_{DS} for both weak and strong conduction region compared to the spin on glass one. This behavior is also related to the reduction of the tunneling length, which improves the subthreshold region characteristics and gm, enhancing gm/I_{DS} in both strong and weak conduction regimes.

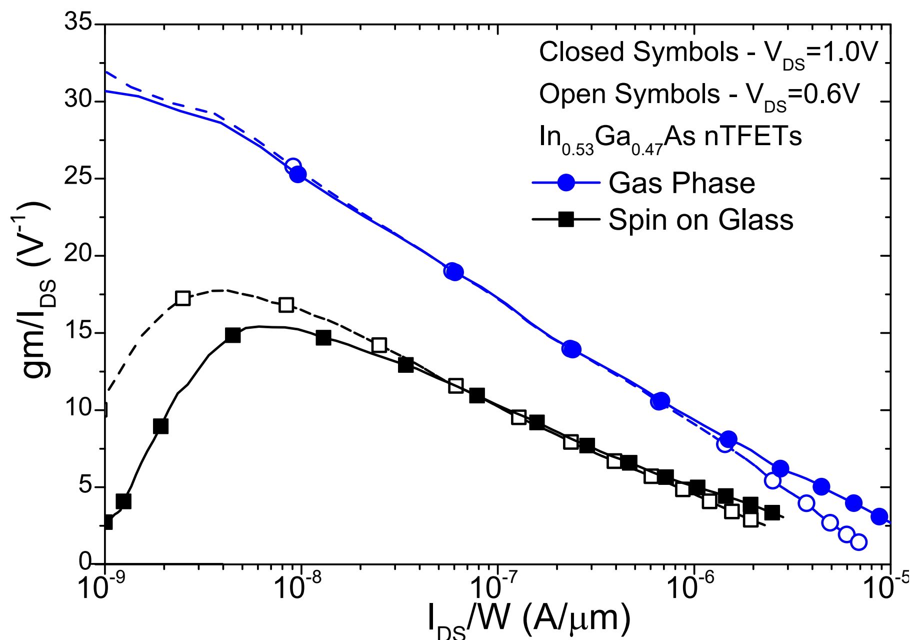

Figure 3. *Experimental transistor efficiency as a function of normalized I_{DS} for $In_{0.53}Ga_{0.47}As$ nTFETs, with different Zn diffusion processes of the source.*

The transconductance (gm) and the output conductance (g_D) as a function of V_{GS} are presented in figure 4. An enhancement in the transconductance in the gas phase device can also be noticed, which is also caused by its lower tunneling length.

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One can observe that for lower V_{GS} values, the influence of V_{DS} on gm is weak, and also the g_D improves.. However, when raising V_{GS}, the influence of V_{DS} on gm increases, also degrading g_D. This behavior can be explained by the fact that the effective energy window of overlap at the source-channel region becomes more dependent on the drain voltage for high V_{GS} values [33], causing g_D degradation and an increase of the influence of V_{DS} on gm. When increasing V_{DS}, the devices become more in the plateau region, reducing (improving) g_D.

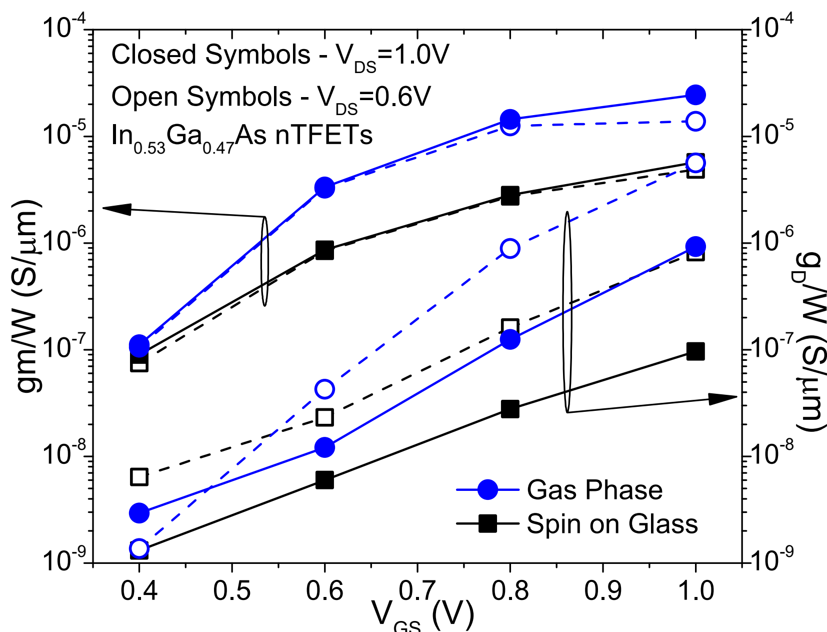

Figure 4. *Experimental normalized gm and g_D as a function of the gate voltage for different Zn diffusion processes of the source.*

The intrinsic voltage gain (A_V), presented in figure 5, was calculated by the gm/g_D ratio. It is noticeable that by enhancing V_{GS}, g_D is also increased, degrading A_V. When comparing both devices with different Zn diffusion processes at the source, one can observe that the gas phase device presents a lower A_V for high V_{GS} due to its significant g_D degradation. However, for lower V_{GS} values it presents a higher A_V due to its more pronounced gm enhancement.

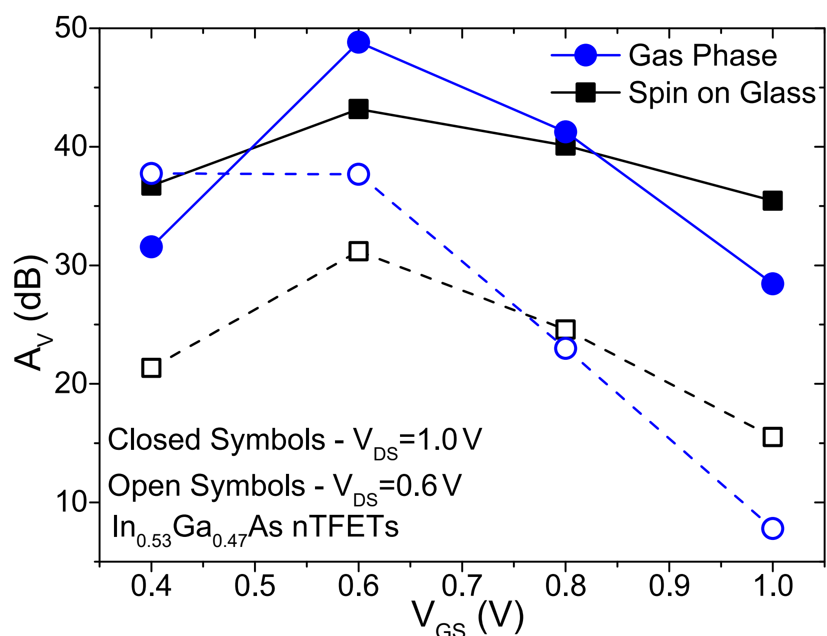

Figure 5. *Experimental A_V as a function of V_{GS} for $In_{0.53}Ga_{0.47}As$ nTFETs, with different Zn diffusion processes of the source.*

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Considering the promising characteristics of the gas-phase-diffused nTFET, the following study, which analyzes the influence of the temperature for different HfO_2 thickness and focusing on the analog parameters, is done only for these devices.

Figure 6 shows I_{DS}/W as a function of V_{GS} for $In_{0.53}Ga_{0.47}As$ with HfO_2 thickness of 2 and 3 nm, at 230, 300 and 430 K, with V_{DS} biased at 1.0V. Considering the effect of the reduction of the HfO_2 thickness, it is possible to observe a slight I_{ON} increase for the 2 nm HfO_2 device caused by the better electrostatic control. This better electrostatic control is also responsible for the improved subthreshold region characteristics, reaching sub-60 mV/dec values at room temperatures.

When the temperature (T) is taking into account, it is necessary to emphasize that TFETs work unlike conventional MOSFETs. The latter present a zero temperature coefficient (ZTC), which is caused, at higher temperatures, by the trade-off between the threshold voltage reduction and the mobility reduction [34]. In TFETs there is no ZTC, as the drain current conduction mechanism (BTBT) increase at higher temperatures due to the bandgap narrowing, resulting in an increase of I_{ON} and not degrading due to mobility degradation observed in MOSFET.

The main current conduction mechanisms in TFETs are BTBT, the dominant current in I_{ON} and TAT and SRH, both dominant currents for I_{OFF}. Although SRH and TAT current mechanisms are directly influenced by the temperature, the BTBT has a smaller temperature dependence, as can be observed in Eq. (1), where the temperature has only an indirect influence in BTBT. On the other hand, SRH and TAT have an exponential increase at high temperatures because they are thermally activated mechanisms. Equations (2) and (3) present the model for the current density of TAT and SRH, respectively [35-37]. As SRH and TAT are exponentially influenced by the temperature and they determine I_{OFF}, I_{OFF} has a higher relative temperature variation compared with I_{ON}, as can be observed in figure 6.

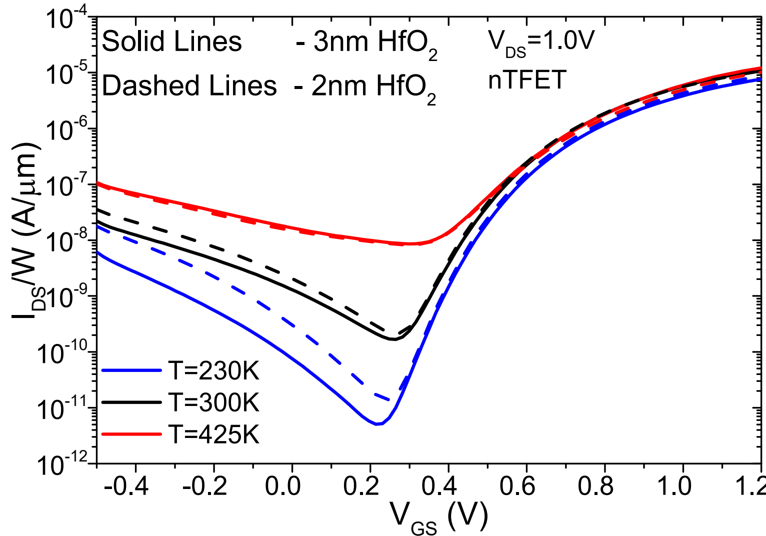

Figure 6. *Experimental normalized I_{DS} as a function of V_{GS} for gas-phase-diffused $In_{0.53}Ga_{0.47}As$ nTFETs, with 2 and 3 nm HfO_2, at different temperatures.*

$$J_{BTBT} \cong . \frac{C1_{BTBT}}{E_g} . e^{\left(-C2_{BTBT} . \frac{E_g^{3/2}}{\xi}\right)} \quad (1)$$

$$J_{TAT} \cong C1_{TAT} . e^{\left(-\frac{\frac{E_g}{2} + (Ed - Ei)}{k.T}\right)} \quad (2)$$

$$J_{SRH} \cong C1_{SRH} . e^{\left(-\frac{\frac{E_g}{2}+(E_d-E_i)}{k.T}\right)} \quad (3)$$

where J is the current density, $C1_{BTBT}$, $C1_{TAT}$ and $C1_{SRH}$ are pre-exponential constants for the simplification of the expressions, E_g is the bandgap, ξ is the total electric field, $C2_{BTBT}$ is an exponential constant for the J_{BTBT} simplification, E_d is the defect energy level, E_i is the intrinsic energy level, and k is the Boltzmann constant.

The activation energy (E_A) represents the logarithm variation of the current as a function of the inverse temperature, and can be used in order to estimate which conduction mechanism is dominant. E_A can be obtained using an Arrhenius plot, shown in equation (4) [25].

$$ln(I_{DS}) = -\left(\frac{E_A}{k \cdot T}\right) + ln(I_0) \quad (4)$$

where I_0 is the off state drain current.

Figure 7 presents E_A as a function of V_{GS}. One can observe that for high V_{GS} the E_A is lower because BTBT becomes the dominant conduction mechanism. In addition, the use of a lower HfO_2 thickness also presents a lower E_A, what can be better observed in the inset of Figure 7, due to its better electrostatic coupling, resulting in a higher BTBT component.

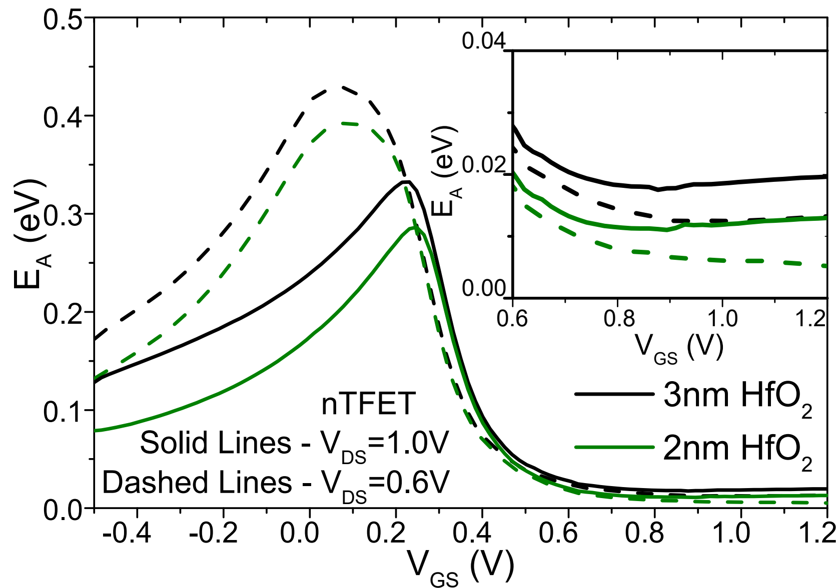

Figure 7. *Experimental activation energy as a function of V_{GS} for gas-phase-diffused $In_{0.53}Ga_{0.47}As$ nTFETs, for two HfO_2 thicknesses, with a V_{DS} of 0.6 and 1.0 V.*

On the other hand, for low V_{GS} values there is a competition of factors among thermally activated mechanisms (TAT and SRH) and the BTBT caused by the ambipolar effect (tunneling between channel and drain) and the conventional BTBT (tunneling between source and channel).

When decreasing V_{GS}, TAT and SRH start to become more dominant, increasing E_A. When decreasing even more V_{GS} the E_A decreases again due to the influence of BTBT on the ambipolar region. This competition of factors can be better observed using numerical simulations, using an Sentaurus Device simulator [38]. The simulations were performed for a uniform $In_{0.53}Ga_{0.47}As$ channel device, considering dopant-dependent SRH, Schenk's non-local TAT, non-local BTBT, and bandgap narrowing models, which parameters where obtained in [39]. Figure 8 presents the simulated I_{DS} as a function of V_{GS}, separating the influence of the thermally activated mechanisms (TAT and SRH) and

BTBT. One can observe that for higher V_{DS}, the lower is the E_A, i.e., the higher is the ambipolar effect. Using thinner HfO_2 has the same influence, increasing BTBT and, consequently, reducing E_A, even in the ambipolar region.

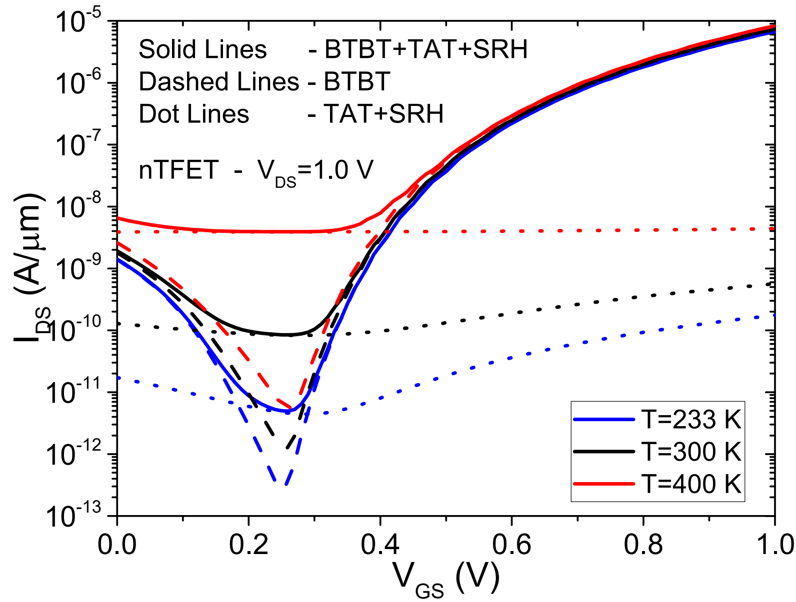

Figure 8. *Simulated normalized I_{DS} as a function of V_{GS} for different temperatures.*

Figure 9 presents gm/I_{DS} as a function of normalized I_{DS} at different temperatures. The inset of this figure presents a zoom of the gm/I_{DS} curve in the strong conduction region. In this region gm/I_{DS} is more dependent on the BTBT mechanism, which has a weak temperature dependence. Additionally, both gm and I_{DS} increase with the temperature, resulting in a slight increase of gm/I_{DS} with temperature.

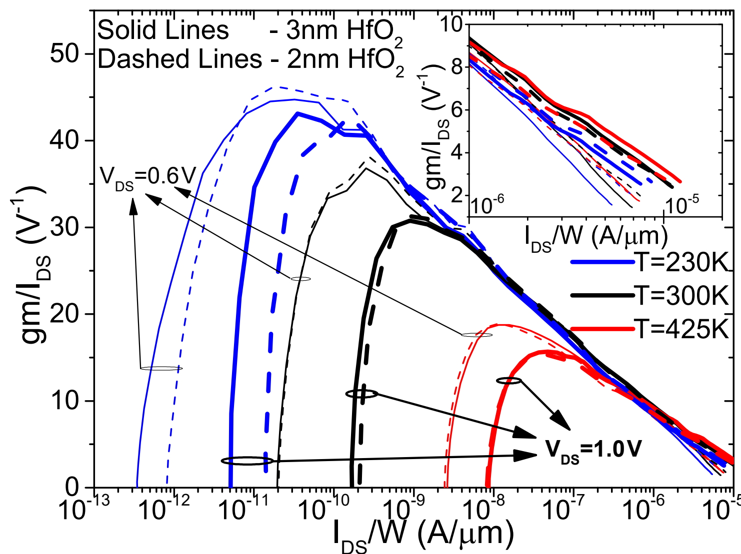

Figure 9. *Experimental gm/I_{DS} as a function of normalized I_{DS} for gas-phase-diffused $In_{0.53}GA_{0.47}As$ nTFETs, for two HfO_2 thicknesses, with a V_{DS} of 0.6 and 1.0 V.*

At the weak conduction region, gm/I_{DS} is inversely proportional to the subthreshold swing (SS), which is presented in figure 10. When the temperature is increased the maximum of the gm/I_{DS} decreases due to the SS degradation, which is caused by the increase of the influence of TAT and SRH mechanisms. One can observe that gm/I_{DS} is slightly higher for the 2 nm HfO_2 device due to its better electrostatic coupling that also improves the minimum SS, reaching values lower than 60mV/dec at room temperature (3 nm – 61mV/dec; 2 nm – 56mV/dec).

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Considering the influence of V_{DS}, it is noticeable that the gm/I_{DS} in the weak conduction region is degraded and shifted in the high I_{DS} direction for high V_{DS} values. This behavior is caused mainly by the increase of the ambipolar current for higher V_{DS}, an effect that can also be observed in figure 10.

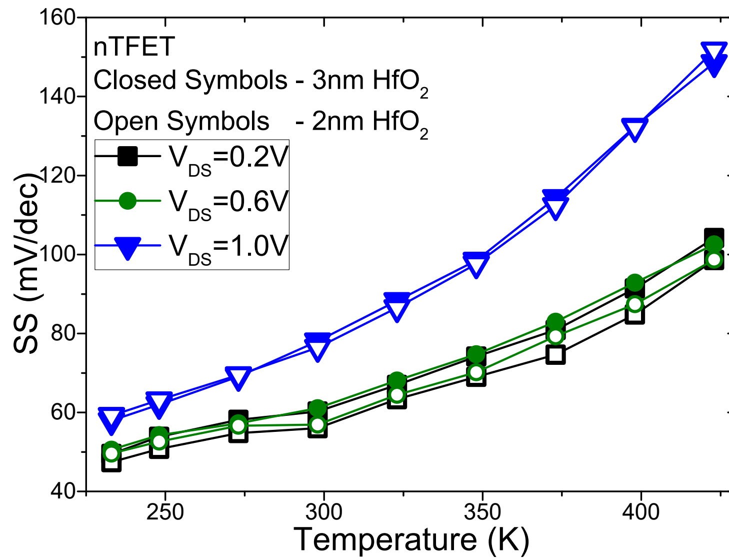

Figure 10. *Experimental subthreshold swing as a function of temperature for gas-phase-diffused $In_{0.53}Ga_{0.47}As$ nTFETs, for both HfO_2 thicknesses, with V_{DS} ranging from 0.2 to 1.0 V.*

The normalized transconductance and the output conductance as a function of temperature are presented in figure 11. One can observe that the gm for the 2 nm HfO_2 devices is slightly higher than the one for the 3nm devices due to its better coupling. When the temperature is raised gm tends to increase, however, at temperatures higher than 400 K the gm presents a decay. This behavior, that is more visible for devices with 2 nm HfO_2, can be related to the presence of series resistance in the devices.

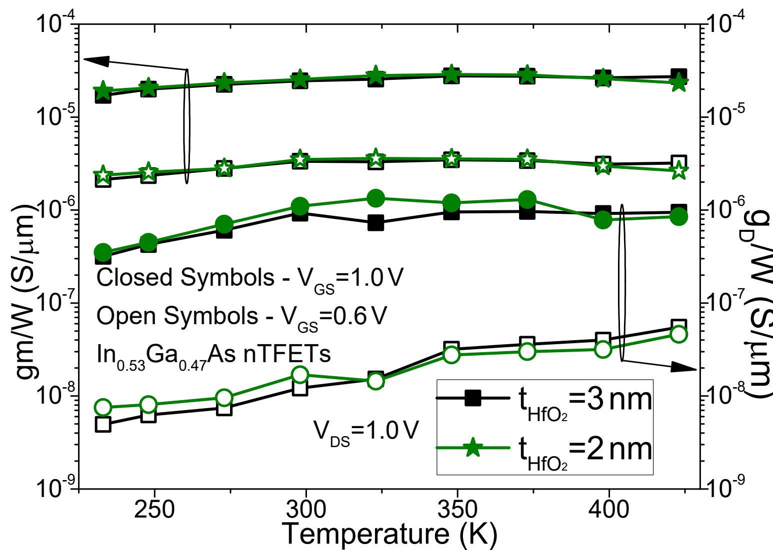

Figure 11. *Experimental normalized output conductance and normalized transconductance as a function of temperature for gas-phase-diffused $In_{0.53}Ga_{0.47}As$ (both EOTs) nTFETs, with a V_{GS} of 0.6 and 1.0 V.*

One can notice that the effect of the temperature on the g_D is higher than on gm. The influence of the temperature on gm is more caused by the increase of I_{DS} at high temperatures, on the other hand, its influence on the g_D is also related with the increase of the BTBT generation rate [16].

Figure 12 presents the experimental A_V as a function of the temperature for both HfO_2 thicknesses, with V_{GS} biased at 0.6V and 1.0 V. The increase of the temperature, which improves gm, but degrades more g_D, results in a net degradation of A_V. One can notice that both devices, biased at V_{GS}=1.0 V give rise to a lower A_V, however, they have also show less variation with the temperature, because in this bias conditions BTBT is dominant.

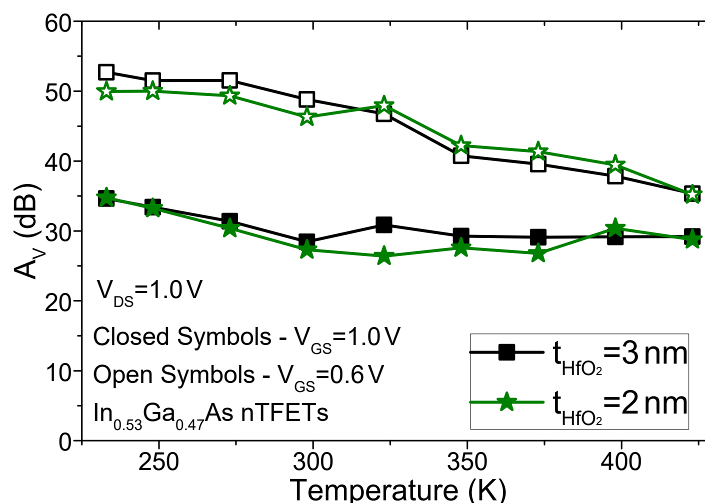

Figure 12. *Experimental intrinsic voltage gain as a function of temperature for gas-phase-diffused $In_{0.53}Ga_{0.47}As$ (both EOTs) nTFETs, with a V_{GS} of 0.6 and 1.0 V.*

Figure 13 presents the A_V as a function of V_{GS} for the 3 nm HfO_2 nTFETs. One can notice a peak in the A_V, which can be related to the point where the E_A (Figure 7) reduces significantly, i.e., where BTBT starts to become the dominant mechanism [40]. Besides the devices present high A_V at this gate voltage range, it is also the point where the temperature strongly degrades A_V. The cause of the strong degradation in this region is due to the change in the conduction mechanism. As the peak is in the region where BTBT starts to become the dominant conduction mechanism, when the temperature is further increased TAT and SRH become more dominant for the same V_{GS}, thereby degrading A_V.

For higher V_{GS} one can observe that the variation of A_V with the temperature reduces. It is, therefore, recommended to use these gate voltages in analog applications covering a broad temperature range.

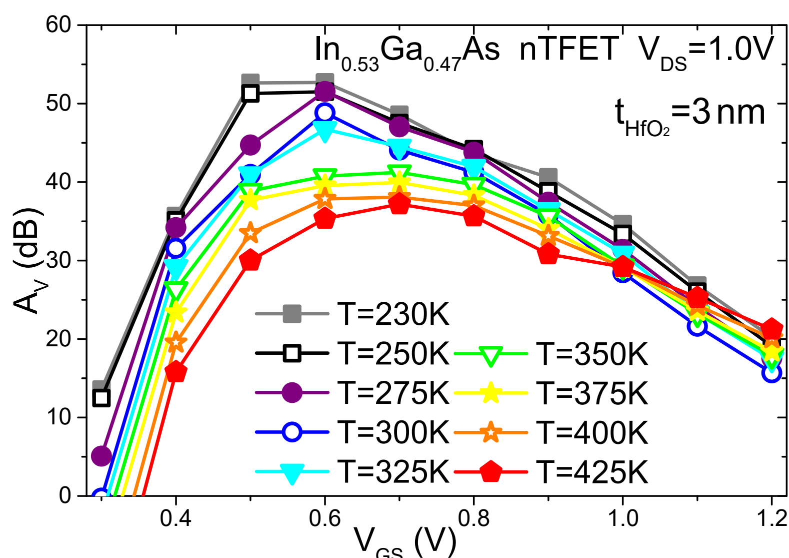

Figure 13. *Experimental intrinsic voltage gain as a function of V_{GS} for gas-phase-diffused $In_{0.53}Ga_{0.47}As$ nTFETs, with a V_{DS} of 1.0 V for 3nm HfO_2*

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Conclusion

A comparative study between the use of spin on glass and gas phase Zn diffusion of the p++ source of InGaAs TFETs was performed. The use of gas phase doping has provided an enhancement of I_{ON}, related to its higher source/channel junction abruptness that reduces the tunneling length and presenting also higher efficiency and intrinsic voltage gain at lower voltages.

The analysis of the analog parameters was done for devices with 3 nm and 2 nm HfO_2 at different temperatures, using only gas phase Zn diffusion at the source. It was observed and proved through simulations that the ambipolar effect is significant for higher V_{DS}. The ambipolar effect degrades SS and consequently gm/I_{DS} in the weak conduction regime, also shifting the gm/I_{DS} peak to higher V_{GS} direction due to the increase of I_{OFF}. The device with 2 nm HfO_2 presents a lower SS (sub 60 mV/dec at room temperature) and higher gm/I_{DS} due to its better electrostatic coupling.

The A_V peak, which is related to the point where the BTBT starts to become the dominant mechanism, is strongly degraded by the increase of the temperature due to the increase of TAT and SRH mechanisms, causing a change in the dominant mechanism in the V_{GS} responsible for the A_V peak.

For higher V_{GS} the intrinsic voltage gain is lower, however, it has shown less sensitivity to temperature variations, being the recommended bias in applications at different temperatures.

Acknowledgments

The authors would like to thank CNPq and FAPESP for the financial support and the support from the imec's Logic Device Program and its Core Partners.

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