Full-quantum modeling of III-V Tunnel-FETs architectures

Performance of Nanodevices

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ABSTRACT. This paper review the device and circuit performance of co-optimized n- and p-type tunnel field-effect transistors (TFETs) integrated on the same InAs/$Al_{0.05}Ga_{0.95}Sb$ platform, using a full-quantum ballistic simulator. Based on 3-D full-quantum simulations, the investigated devices feature steep subthreshold slopes and relatively high ON-state currents, and are combined to realize an inverter. Benchmarking against aggressively scaled CMOS logic based on multi-gate architectures highlights the potential of the proposed TFET implementations to perform up to 10× and 100× faster for I_{OFF} = 5nA/um and 10 pA/um, respectively, at very low supply voltage V_{DD} = 0.25V, for equal levels of static power dissipation. Afterwards, a simulation study on the impact of interface traps and strain on the I–V characteristics is carried out, in order to capture the effect of interface/border traps on the device electrostatics. The effect of an experimental D_{it} distribution of a high-*k* gate stack on InAs is investigated. Unfortunately, traps induce a significant reduction of the ON-state current. However, it turns out that localized strain at the source/channel heterojunction caused by lattice mismatch is able to induce a performance enhancement for the n-type TFET, with respect to the ideal device, even in the presence of traps. On the contrary, for the p-type one, a current degradation ~ 18% is observed.
KEYWORDS. III–V materials, heterojunction, subthreshold slope, interface traps (ITs), quantum transport, strain, tunnel FETs (TFET).

1. Introduction

Aggressive scaling of device dimensions is currently being pursued by multigate field-effect transistors [Auth 12], whereas transistors exploiting different operating principles are required to further reduce the supply voltage V_{DD}. Tunnel FETs (TFETs) are considered to be one of the most promising alternatives to the conventional CMOS technology, in the quest for supply voltage reduction and power containment [Lu 14], [Ionescu 11]. TFETs are especially interesting due to their peculiar injection mechanism, that makes it possible to achieve subthreshold swings (SS) lower than 60mV/dec at room temperature and, thus, higher ON-state currents (I_{ON}) at very low supply voltages.

Major challenges associated with the TFET architecture include: 1) reaching acceptable I_{ON} levels; 2) suppressing ambipolar effects, affecting the off-state performance; 3) dealing with the superlinear onset and high saturation voltage of the device output characteristics [Pal 11]; 4) reducing Miller effects associated with the typically high gate–drain capacitance C_{gd} [Mookerjea 11]; and, 5) cointegrating simultaneously optimized n- and p-type devices. More generally, literature on p-TFETs is relatively scarce compared to that on n- TFETs, and the two device types are often studied separately.

There is wide consensus on the use of III-V based heterostructures with staggered or broken-gap lineups to boost the ON-state current and realize a complementary technology platform, whereas a careful optimization of the device geometry, doping levels, and gate-stack is required to improve performance [Baravelli 14-I]. Furthermore, for digital applications, slope and I_{ON} are not the only relevant parameters to be considered. Voltage transfer characteristics (VTC), voltage gain and switching current, as well as rise and fall times, contribute to circuit-level performance. In addition, interface states may have a significant impact on the drain current, degrading I_{ON} and the subthreshold slope [Passlack 10], [Lin 11]. In this respect, the achievement of low interface and border trap densities is one of the main technology challenges to be addressed [Pala 12].

However, for III–V-based TFETs, it is possible to boost the device performance, taking advantage of appropriate strain conditions [Visciarelli 16].

This paper review the device and circuit performance of co-optimized n- and p-type tunnel field-effect transistors (TFETs) integrated on the same InAs/$Al_{0.05}Ga_{0.95}Sb$ platform. In contrast with the largest part of available literature, a full-band quantum simulation approach is used in this paper to properly account for quantum effects, which strongly influence TFET behavior and, thus, circuit performance. Afterwards, performance of the investigated circuit blocks is compared with best-case predictions for aggressively scaled CMOS logic, based on multi-gate architectures. Afterwards, the investigation is here extended to take into account the combined effect of traps and strain on the device characteristics.

The paper is organized as follows. The physical model used for the investigation is described in Section 2. The TFET-based platform and the proposed inverted implementations are highlighted in Section 3 and 4, respectively. The combined effect of interface traps and localized strain is investigated in Section 5. Concluding remarks are given in Section 6.

2. Physical model

Numerical simulations are carried out using a four-band **k•p** Hamiltonian [Vurgafmann 01] in a fully 3-D framework, to accurately model multiband effects and the complex band structure of our devices. A non-equilibrium Green function (NEGF) formalism is employed for transport description within the ballistic approximation [Lake 97], which is expected to be a reasonable assumption for the gate lengths investigated here, due to the high electron mobility and long mean free path of III–V materials. The NEGF module is self-consistently coupled with a 3-D Poisson solver for electrostatics computation.

The effect of strain is included using the Pikus–Bir formalism with Bahder extensions [Bahder 90], [Bahder 93] for zinc-blende crystals. With such an approach, a strain-tensor-dependent matrix Hstrain is added to the basis **k•p** Hamiltonian of the unstrained material. The strain-dependent matrix includes deformation potential constants and k-dependent terms, which couple the different bands with strain among them. Material parameters are taken from [Vurgafmann 01], and spurious solutions in the gap are eliminated using the procedure proposed in [Foreman 01]. Zero wave function penetration in the insulator is assumed. Contact resistances are not considered either, as their impact is strongly dependent on the actual fabrication technology, which is beyond the scope of this paper.

In order to capture the effect of interface/border traps on the device electrostatics, consistently with carrier degeneracy and ballistic transport, the classical Shockley–Read–Hall theory can be properly generalized. The model assumes that traps are of both acceptor and donor type, located at the semiconductor/oxide interface, and uniformly distributed over the interface area. Only the electrostatic effect of traps is considered via Poisson's equation. At every NW cross section, the occupation probability of traps at every energy E_t in steady state is determined from the balance of electrons and holes emission and capture processes. The electronic states generated by wave function propagation from the source and the drain leads are separately considered, consistently with the ballistic NEGF picture. The derivation of the trap model can be found in [Visciarelli 17-TED].

3. Device structure and technology platform assessment

Heterostructures are exploited to achieve satisfactory I_{ON} levels with the TFET architecture, and promising experimental studies have been reported on III–V antimonide compounds. Baravelli et al. [Baravelli 14-I] have indicated InAs/$Al_{0.05}Ga_{0.95}Sb$ as a suitable material pair for cointegration of n- and p-type devices with similar dimensions and opposite choices for the source and channel/drain materials. The TFETs considered here are a modified version of the 7-nm-side platform described in [Baravelli 14-I], and feature a gate length of 20 nm.

Device sketches are shown in Fig. 1, and feature a gate-all-around nanowire geometry with square cross section.

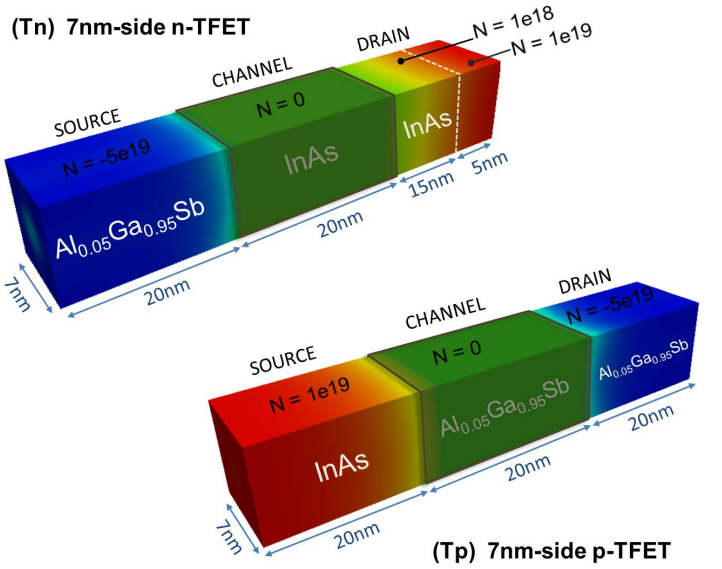

Figure 1. *Pictorial view of the n-type (Tn) and p-type (Tp) heterojunction TFETs based on the InAs/Al0.05Ga0.95Sb material pair. Doping concentrations are expressed in cm-3 and abrupt profiles are assumed. A non-uniform drain doping is used to reduce ambipolarity in Tn. The gate dielectric is Al2O3 with an equivalent oxide thickness EOT = 1nm.*

Both devices were designed to meet the International Technology Roadmap for Semiconductors OFF-state current specification of 5 nA/μm at V_{DD} = 0.4 V, with sub-60 mV/decade minimum and average subthreshold slope, together with relatively high ON-currents (I_{ON} ~ 350μA/μm for Tn, and I_{ON} ~ 75 μA/μm for Tp) [Baravelli 14-II]. Turn-on curves computed at V_{DD} = 0.4 V for the TFETs in Fig. 1 are shown in Fig. 2(a), where currents are normalized by the device side. The curves are shifted by the V_{GS} value (V_{OFF}) at which the corresponding I_{OFF} level is reached, to compare the device performance for equal static power consumption. Both devices exhibit sub-40 mV/decade minimum SS [Fig. 2(b)] and sub-60 mV/decade average subthreshold slopes (SS_{av}) [Fig. 2(c)], which are sustained for about three decades of drain current [Fig. 2(d)]. This is combined with relatively high I_{ON} levels at 0.4 V supply voltage, especially for the n-TFET [Fig. 2(e)].

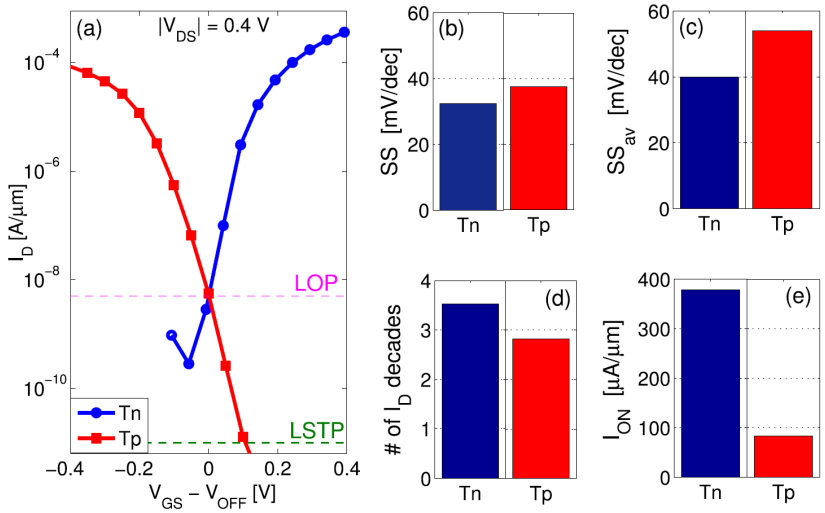

Figure 2. *(a) Simulated I_D–V_{GS} curves at $|V_{DS}|$ = 0.4 V for the TFETs in Fig. 1 (normalized by device side for consistency with quantization-induced charge distribution). LSTP (10 pA/μm) and LOP (5 nA/μm) specs on I_{OFF} are indicated. Curves are shifted by the respective V_{OFF}, i.e., the V_{GS} at which I_D = 5 nA/μm. Corresponding device performance is evaluated in terms of (b) minimum SS, (c) average subthreshold slope, SS_{av}, (d) number of current decades over which SS_{av} is computed, and (e) I_{ON} at V_{DD} = 0.4 V.*

It is worth noting that the output curves show a high output conductance at low V_{DS} for both the n- and p-type devices (see Fig. 4 in [Baravelli 14-II]).

4. TFET-based inverter design

This technology platform has been considered as potential competitor of a conventional CMOS logic. The off-current has been fixed at 5 nA/μm and two different supply voltages have been investigated, namely V_{DD} = 0.4 V and 0.25 V.

To compensate for the current difference between the n- and p-type devices shown in Fig. 2, four p-type devices connected in parallel are considered. TFETs are benchmarked against FinFET-based CMOS logic projected to the 10-nm technology node. The assumed FinFETs exhibit 14-nm gate length, 9-nm fin width, 21-nm fin height, and are simulated in SPICE using PTM-MG [Sinha 12]. The work functions in PTM model cards are adjusted to make I_{OFF} and, thus, static power dissipation, identical for the two device types.

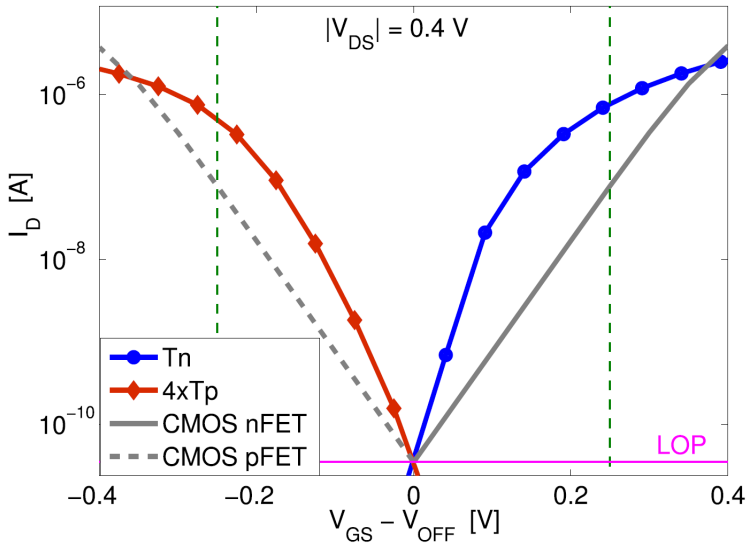

Figure 3. *ID–VGS curves of 4×Tp and 1×Tn compared with those of 10-nm-node CMOS FinFETs computed with PTM-MG SPICE models [Sinha 14]. The WFs in PTM model cards are adjusted to make IOFF = 5 nA/μm and, thus, equal static power dissipation. The FinFET subthreshold slope is about 75 mV/decade. Dashed vertical lines: TFET advantage when VDD is reduced from 0.4 to 0.25 V.*

Turn-on curves are compared in Fig. 3 with those obtained from n- and p-type FinFET simulation (4×Tp and 1×Tn). TFETs are seen to provide considerably improved subthreshold performance, and the two architectures exhibit a break-even point for current drive at $|V_{GS} - V_{OFF}|$ = 0.35 V, so that FinFETs have some I_{ON} advantage at V_{DD} = 0.4 V. As a consequence, CMOS logic is faster than its TFET counterpart, both under self-loading or constant-loading conditions, as demonstrated in Fig. 4 (a) and (b), respectively. Results for the self-loading case are further motivated by the higher effective load of TFET inverters due to the Miller contribution, which is instead assumed to be negligible for the CMOS logic. Under self-loading conditions, an equal inverter stage in a chain configuration is considered. Miller effects are accounted for through an additional load capacitance equal to 2 × C_{gd}, with the estimated gate-drain capacitance $C_{gd} \approx 0.8 \times C_g$ (gate capacitance), which is a reasonable assumption for III–V TFETs [Mookerjea 09]. This leads to an effective load of 2.6 × C_{in} with C_{in} the total input capacitance. The C_{gd} component is instead neglected in the constant loading condition. Rise and fall times $t_{r,f}$ are estimated in response to an instantaneous voltage step, and are computed by integrating the device output characteristics at V_{GS} = 0 V or $|V_{GS}| = V_{DD}$ [Baravelli 14-II].

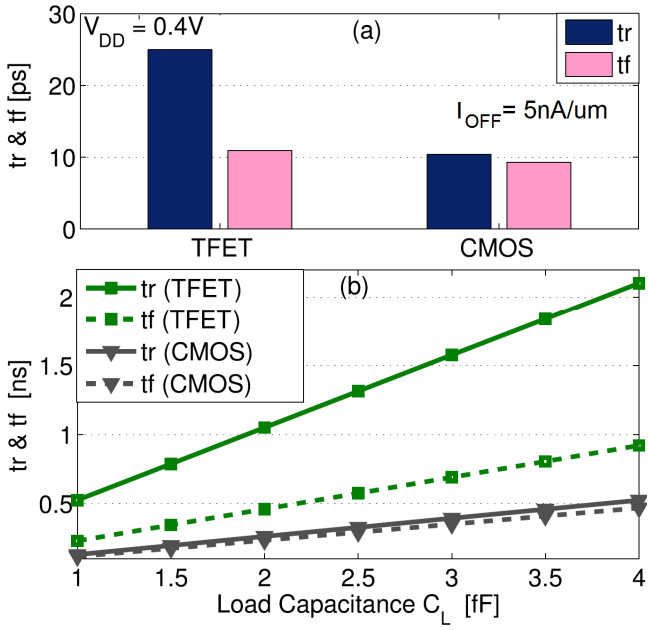

Figure 4. *Rise and fall times of TFET-based inverter and of a 10-nm CMOS-based inverter, operating at I_{OFF} = 5 nA/μm, and V_{DD} = 0.4 V. CMOS logic is faster than TFET in both (a) self-loading and (b) constant loading, because it provides a higher drive current at V_{DD} = 0.4 V, and is not significantly affected by the Miller effect.*

On the other hand, Fig. 3 indicates a potential advantage of TFETs at sub-0.35 V supply voltage. More specifically, the advantage in current drive is over 10× at V_{DD} = 0.25 V. As demonstrated in Fig. 5, TFET logic is predicted to be about 10× and 7× faster than CMOS logic under self-loading and constant loading conditions, respectively.

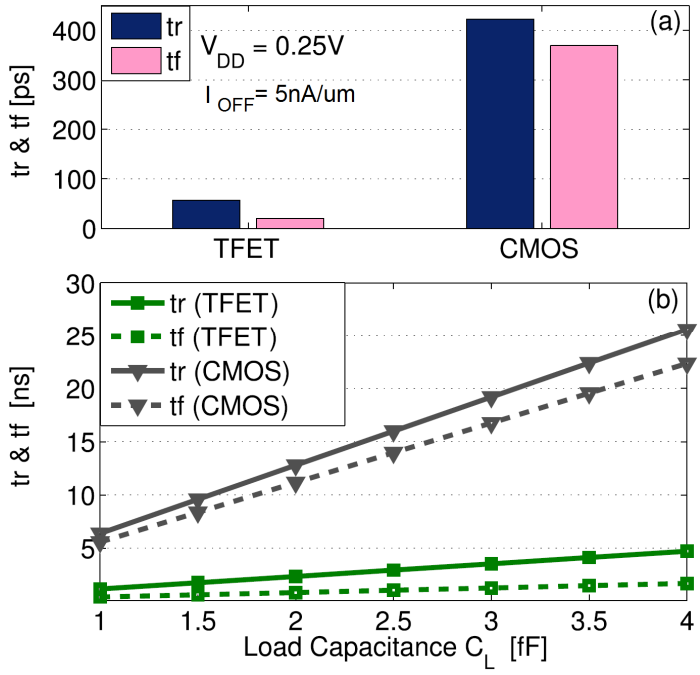

Figure 5. *Rise and fall times of a TFET-based inverter and of a 10-nm CMOS-based inverter, operating at I_{OFF} = 5 nA/μm, and V_{DD} = 0.25 V. TFET logic is substantially faster than CMOS under both self-loading and constant loading.*

Finally, a similar investigation has been carried out for I_{OFF} = 10 pA/um at V_{DD} = 0.25 V. The decrease of the supply voltage ensures a reduction of the ambipolar behaviour that allows to reach the LSTP I_{OFF} target. Results are summarized in Table I in terms of static power dissipation, TFET to CMOS speedup under self-loading [Speedup (Cin)] and constant loading [Speedup (CL)] conditions. Static power consumption is equal

for the two technologies as a design constraint, whereas other figures of merit are defined so that values greater than 1 indicate advantage of TFET over CMOS.

	I_{OFF} = 5 nA/um V_{DD} = 0.4 V	I_{OFF} = 5 nA/um V_{DD} = 0.25 V	I_{OFF} = 10 pA/um V_{DD} = 0.25 V
P_S (TFET, CMOS)	14 pW	8.75 pW	0.0175 pW
Speedup (C_{in})	0.55×	10×	353×
Speedup (C_L)	0.32×	7.45×	105×

Table I. *Performance comparison of TFET and CMOS logic.*

Table I clearly shows the potential of the TFET technology to perform substantially faster than a best-case CMOS implementation at 0.25 V supply voltage, for equal levels of static power consumption (P_S) in line with the ITRS requirements.

5. Impact of Traps and Strain

Interface states may have a significant impact on the drain current, degrading both I_{ON} and subthreshold slope [Passlack 10], [Lin 11]. In this respect, the achievement of low interface and border trap densities is one of the main technology challenges to be addressed [Pala 12]. For III–V-based TFETs, it is possible to boost the device performance, taking advantage of appropriate strain conditions [Visciarelli 16]. It was also shown that the trap energy levels remain unchanged in the presence of an external strain [Kim 11]. The detailed investigation of the effect of strain on InAs/GaSb heterojunction devices has been reported in [Visciarelli 17-SSE], where it was demonstrated that the application of an uniform biaxial tensile strain across the device cross section can provide the largest performance improvement. In principle, uniformly distributed strain across the whole structure could be achieved taking advantage of the lattice mismatches between the structure and the underlying substrate. Unfortunately, the application of a uniform strain along the whole device structure is especially challenging from the fabrication perspective. More reasonably, strain will be localized at the heterojunction because of lattice mismatch [Visciarelli 17-TED].

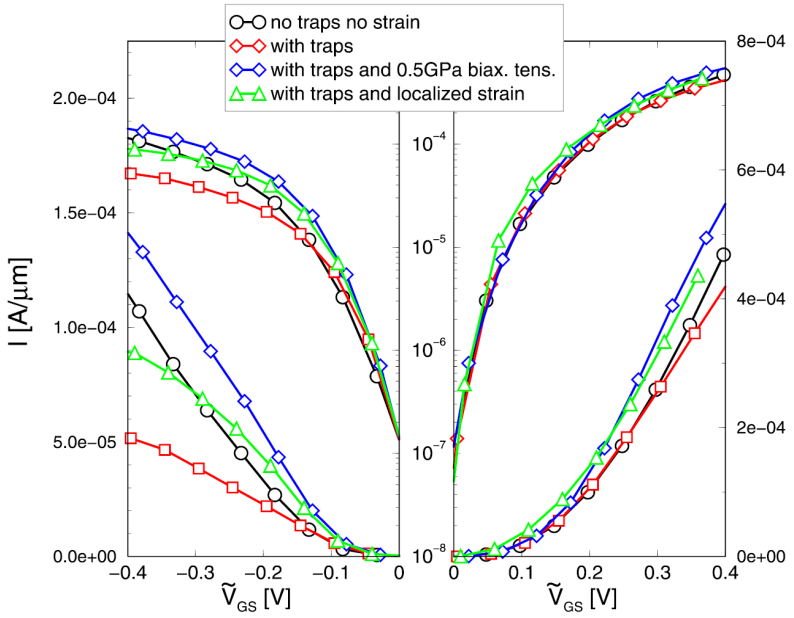

Figure 6. *I_{DS} versus V_{GS} at $|V_{DS}|$ = 0.4 V without ITs (black circles), with traps (red squares), with uniform biaxial tensile strain of 0.5 GPa (blue diamonds), and localized strain (green triangles). (a) Tp. (b) Tn. Currents are normalized to the NW side, and the curves are V_G-shifted in order to have I_{ON} = 100 nA/µm at V_{GS} = 0 V.*

In the absence of experimental data on strain maps in AlGaSb/InAs NW TFETs, we took advantage of process simulation results found in [Verreck 16] for a GaSb/InGaAs double-gate device, where the InGaAs region is assumed to be grown pseudomorphically on a relaxed GaSb. In order to reproduce this process simulation, we used a layer-dependent strain applied along the device cross section, with a strain map similar to that shown in [Verreck 16].

The I–V curves obtained considering traps and this localized strain caused by lattice mismatch are reported in Fig. 6. Curves are V_{GS}-shifted to match an I_{OFF} = 100 nA/µm at V_{GS} = 0 V. Currents with traps (red squares) are smaller than the ideal ones (black circles), but still steadily increasing with V_{GS}, indicating that a Fermi-pinning condition in the channel is not reached for the biases here considered. The current reduction is of ~60% for Tp, and ~20% for Tn.

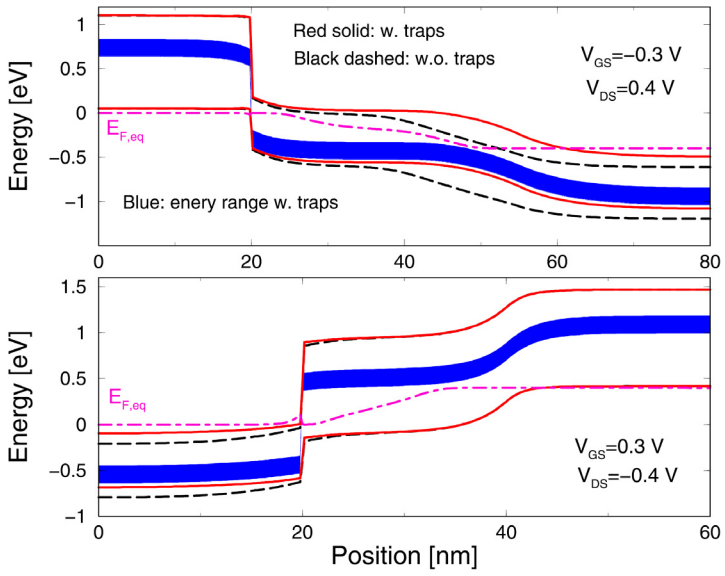

Figure 7. *Conduction and valence subband profile for Tn (top) and Tp (bottom). VGS values are chosen in order to bias our devices in subthreshold. VDS = 0.4 V. Black dashed lines: without traps. Red solid lines: with traps. The energy interval where trap levels are located is highlighted (blue region). Magenta dashed curve: equivalent Fermi level.*

For Tn, the current reduction caused by traps can be understood plotting the conduction and valence subband profiles [Fig. 7 (top)]. Trapped electrons in the channel lift up the conduction subband energy, hence increasing the tunneling distance. One positive side effect is the electric-field decrease at the channel/drain junction, responsible for ambipolar behavior. As for Tp, the situation is different, because the trapped charge affects the n^+ source more than the channel/drain region. This is due to the fact that the trap distribution measured in [Wang 15] is of acceptor type [Fig. 7 (bottom)]. Indeed, for every applied voltage, traps in the channel and drain regions of Tn are always filled, since the trap energy levels are always below the equivalent Fermi level [see Fig. 6 (magenta dashed curve)]. The opposite happens for Tp, where the equivalent Fermi level is above the trap level in the source region, regardless of the applied gate voltage. With localized strain a performance improvement is obtained. For Tn, an I_{ON} ~ 500 µA/µm higher than that exhibited by the fresh device is obtained, with SS = 32 mV/decade. For Tp, lattice mismatch is unable to completely recover the trap-induced I_{ON} degradation, with I_{ON} ~ 90 µA/µm and SS = 54 mV/decade. It is worth noting that for this localized strain, the bandgap is modified only near the heterojunction, leaving the band edges near the source/drain contacts unaltered (same degeneracy).

The subband profiles and trap energy level diagrams with this localized strain are reported in Fig. 8 at V_{GS} = −0.3V for Tn and at V_{GS} = 0.3V for Tp ($|V_{DS}|$ = 0.4 V), to be compared with Fig. 6 for the case with traps but without strain. The main point here is that, as a consequence of the bandgap decreasing, only at the

source/channel interface, the tunneling window increases, changing from a staggered- to a broken-gap heterojunction, whereas the source/drain regions near the contacts remain unchanged.

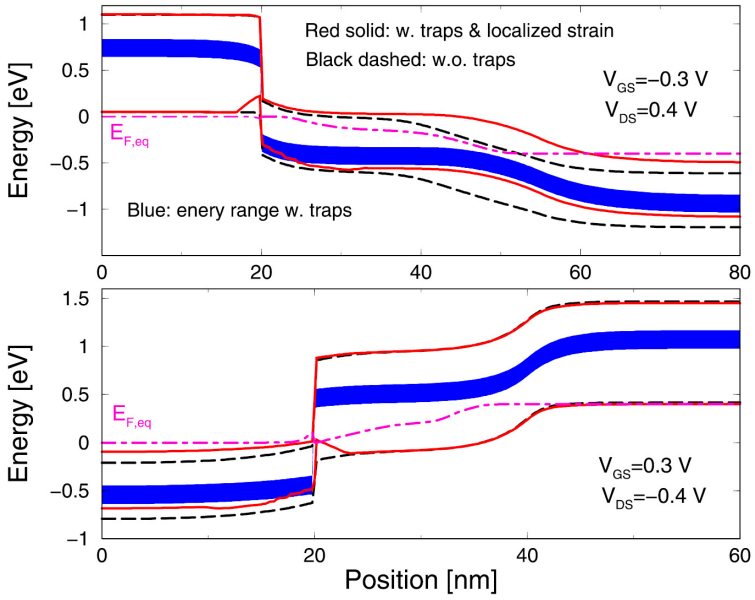

Figure 8. *Conduction and valence subbands profile in subthreshold for TFETs Tn (top) and Tp (bottom). Black dashed lines: with no traps. Red solid lines: with traps and localized strain. The energy interval where trap levels are located (blue region) is reported as well. Magenta dashed curve: equivalent Fermi level.*

6. Conclusions

TFET technology has been reviewed in this paper as a potential alternative to conventional CMOS-based logic for near-future low-voltage/low-power applications. The proposed solutions integrate n- and p-type heterojunction TFETs with similar dimensions on a same InAs/$Al_{0.05Ga0}$.95Sb platform. Full-quantum simulations have been employed to investigate static and dynamic performances of inverter blocks compatible with ITRS low-operating power requirements of the off-state leakage, i.e. 5nA/um. Results are compared with the best-case predictions for aggressively scaled CMOS logic based on multigate architectures. It is found that TFET implementations have potential to perform up to 10× and 100× faster than CMOS for I_{OFF} = 5nA/um and 10 pA/um, respectively, at very low supply voltage V_{DD} = 0.25 V, for equal levels of static power dissipation. Afterwards, realistic trap energy distribution and strain conditions have been taken from the literature. However, it turns out that localized strain at the source/channel heterojunction caused by lattice mismatch is able to induce a performance enhancement for the n-type TFET with respect to the ideal device, even in the presence of traps. On the contrary, for the p-type one, a current degradation is still observed.

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